CURRICULUM VITAE – Gianluca Setti

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1. Brief Overview

Gianluca Setti
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Electrical and Computer Engineering (ECE) Program
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1.1 Research Interests

- Switching Power Converters (for Integrated Systems and IoT Nodes)
- Biomedical Circuits, Systems and Signal Processing
- Nonlinear Signal Processing and Statistical Algorithms for (Integrated) Systems Optimization (DS-CDMA Communication, EMI reduction)
- Embedded Systems Security
- Internet of Thing and Edge Computing (Compressed Sensing for IoT nodes: Algorithms, Architectures and Implementation)
- Information Processing in Artificial Neural Networks
- Machine Learning for Signal and (Big) Data Processing, Anomaly Detection & Predictive Maintenance

1.2 Education

- Ph.D. in Electronic Engineering and Computer Science, 1997, University of Bologna, School of Engineering, Bologna, Italy.
- Dipl. and M.S. (cum laude) in Electronic Engineering, 1992, University of Bologna, School of Engineering, Bologna, Italy.

1.3 Academic Positions

- November 2022-Present: King Abdullah University of Science and Technology, **Dean**, Division of Computer Electrical Mathematical Science and Engineering (CEMSE) & **Professor**, Electrical and Computer Engineering
- December 2017-November 2022: **Professor**, Politecnico di Torino, Department of Electronics and Telecommunications (DET), Turin, Italy.
- December 2008-December 2017: **Professor**, University of Ferrara, Department of Engineering, Ferrara, Italy.
- June 2011, **Visiting Professor**, University of Washington, Seattle, WA, USA
- July-August 2010, **Visiting Professor**, University of Washington, Seattle, WA, USA
- September-October 2008: **Visiting Professor**, University of Washington, Seattle, WA, USA
- August 2007: **Visiting Scientist**, IBM T. J. Watson Research Center, Hawthorne, NY, USA
- November 2001 – November 2008: **Associate Professor**, University of Ferrara, Department of Engineering, Ferrara, Italy.
- April 2000 - Present: **Faculty Member**, University of Bologna, Advanced Research Center on Electronics Systems for Information and Communication Technologies (ARCES), Bologna, Italy.
- July 2005: **Visiting Professor**, Summer Research Institute, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland.
- August 2004: **Visiting Professor**, Institute of Nonlinear Science, University of California San Diego (UCSD), San Diego, California, USA.
- July 2002: **Visiting Professor**, Summer Research Institute, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland.
- October 1998 - October 2001: **Assistant Professor**, University of Ferrara, Department of Engineering, Ferrara, Italy.
- March 1997 - October 1998: **Lecturer**, University of Ferrara, School of Engineering, Ferrara, Italy.
- May 1994 - July 1995: **Visiting Researcher**, Laboratory of Nonlinear Systems (Head: Prof. Martin Hasler), Communication and Computer Science Faculty, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland.

2. Selected Awards and Leadership Positions ***(detailed description following)***

2.1 AWARDS

1. **Fellow of the IEEE**, *for contributions to application of nonlinear dynamics to communications, signal processing, and information technology*, 2006.
2. **IEEE Transactions on Biomedical Circuits and Systems Best Paper Award**, 2019, for the article "Hardware-Algorithms Co-Design and Implementation of an Analog-to-Information Converter for Biosignals Based on Compressed Sensing," *IEEE Transactions on Biomedical Circuits and Systems,* vol. 10, n. 1, pp. 149-162.
3. **IEEE CAS Society Guillemin-Cauer Award**, 2013, for the article "Rakeness in the design of Analog-to-Information Conversion of Sparse and Localized Signals," *IEEE Transactions on Circuits and Systems – Part I*, vol. 59, n. 5, pp. 1001 – 1014, 2012.
4. **IEEE CAS Society Darlington Award**, 2004, for the article "Spectral properties of chaos-based FM signals: Theory and simulation results," *IEEE Transactions on Circuits and Systems – Part I,* vol. 50, pp. 3-15, 2003.
5. **IEEE CAS Society Meritorious Services Award**, 2013, which honors the individual with exceptional long-term service and dedication to the interest of CAS Society, received for *extraordinary leadership in improving timeliness, technical quality, and the reputations of IEEE TCAS-I and IEEE TCAS-II*.
6. **Distinguished Lecturer**, IEEE Circuits and Systems Society, 2015-2016.
7. **Distinguished Lecturer**, IEEE Circuits and Systems Society, 2004-2005.

2.2 LEADERSHIP/MANAGEMENT

IEEE

1. **IEEE Vice President for Publication Services and Products**, (VP-PSP) 2013 and 2014 (two consecutive elected terms). This was **the first time in the history of the IEEE** in which **a Scientist not from North America** has been elected to this role.
2. **President**, **IEEE Circuits and Systems Society**, (CASS) 2010 (President-elect in 2009, Past-President in 2011). This was the first time in the history of CASS that a scientist of an Italian institution was elected in this position
3. **Editor-in-Chief,** PROCEEDINGS OF THE IEEE*,* 2019-present (reappointed for a second 3-year term in 2022). The Proceedings of the IEEE is the Flagship publications of the IEEE and its editorial board is composed only by IEEE Fellows. **I am the first non-US scientist** to be selected for the role of EiC in the history of the journal, which can be traced back to its early beginnings in 1909 (when it was known as the Proceedings of the Wireless Institute).
4. **Editor-in-Chief**, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I, 2008-2009 and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-II, 2006-2007.
5. **Co-Chair, General,** *IEEE International Symposium on Circuits and Systems (ISCAS2018)*, Florence, Italy, 2018 (second time that ISCAS was organized in Italy since the early 80').

Department/University

6. **Dean**, Computer Electrical Mathematical Science and Engineering Division, KAUST, 2022-now. Responsible of the administration of 69 faculty and 27 permanent staff members with a research budget of ~$90M.
7. **Rector's Delegate for Research Quality Evaluation,** Politecnico di Torino, 2019-present. Responsible for the research assessment of the entire university.
8. **Associate Department Chair for Research**, Department of Electronics and Telecommunications (DET), Politecnico di Torino, 2019-present.
9. **Associate Department Chair for Internationalization and Students Mobility**, Department of Engineering (DE), University of Ferrara, 2012-2016.
10. **Coordinator of the Project**, 2002-2010, European Ph.D. Program on Information Technology (EDITH)
11. **Chair**, **Group of Experts for Evaluation (GEV)**, 2015-2017, for the area of Information and Industrial Engineering (GEV09), of the Evaluation of Research Quality Exercise 2011-2014 (VQR2011-2014) for all Italian Universities, for the Italian National Agency for Evaluation of Universities and Research Institutes (ANVUR).

3. Academic Management

1. **Dean**, Division (equivalent to a School) of Computer, Electrical, Mathematical Science and Engineering (CEMSE), KAUST, 2022-present. A short description of my main responsibilities as well as the most significant results achieved over the first year in this role are reported below:
   a. ***Academic Leadership.*** I oversee the development and implementation of academic programs, curricula, and research initiatives in all areas fields related to CEMSE[1]. In this role, I supervise the activities of the *Associate Dean (AD) for Students* and the *Associate Dean for Research*, and coordinate the operation of the *Chairs* of the four Programs (Departments) of Computers Science (CS), Electrical and Computer Engineering (ECE), Applied Mathematics and Computational Science (AMCS), and Statistics (STAT). I am also an ex-officio member of the:
      1) Academic Curriculum Committee (ACC), approves and oversees all current programs, eventual changes to the aforementioned and creation of any new ones at KAUST;
      2) Academic Council, in charge of creation and execution all policies and matter of general concern to the university community at large;
      3) Academic Leadership Committee (ALC), which includes the President, Provost, the Deans of the 3 KAUST Divisions, plus Dean of Graduate Affairs. The ALC is in charge of planning and execution of strategic directions for KAUST as a whole.

      MAIN RESULTS. I succeeded in starting, finalizing or continuing several innovative academic programs in the framework of "lifelong learning". More specifically:
      1) *MS in Data Science for Employees of Saudi Aramco*. When I joined KAUST the first edition of the Master's program had already been initiated and had encountered a number of challenges in terms of teaching activity coordination. Under my leadership, a solution as created for the above, which allowed to satisfactory conclude the program. Building on this positive result, **I was able to convince Aramco of the benefits of the program for their employees, and creation of on-going, annual program thereafter**. The new cohort will start in Fall 2024;
      2) *Master of Professional Studies (MPS) in Artificial Intelligence for Employee of Saudi Ministry of Interior.* The Associate Dean for Students and I developed this program as a new kind of degree at KAUST – i.e., a Master of Professional Studies (MPS) – specifically targeted towards lifelong learning. The program is currently ongoing and the first semester has been successfully completed;
      3) *MPS in Cybersecurity for Employees of the Saudi Ministry of Interior*. This MPS is currently under development, and at the approval stages within KAUST and will be offered starting in Fall 2024.
      4) *Post Graduate Diploma in Data Science and Analytics and in Industrial Microelectronics*. I contributed to the creation of two curricula (out of four in total) of the Post Graduate Diploma which was offered for the first time at KAUST starting in Fall 2023;
      5) *MS in Technology, Innovation and Entrepreneurship (TIE)*. I am a member of the Steering Committee and contributed to the design of the new TIE program, which aims at nurturing a new generation of innovative thinkers and entrepreneurs. The program emphasizes the fusion of cutting-edge technology and entrepreneurial spirit to foster **creativity, problem-solving skills, and hands-on experience**. Central to the program is its project-based learning approach, where students engage in iterative product development cycles, combining theoretical knowledge with practical applications. The program take advantage of the newly established KAUST Hub in Shenzen (China), where part of the program will be held, to rely on the entrepreneurial ecosystem offered there;
      6) *Dual MS/PhD Degree Programs between KAUST and Selected Foreign Institution.* I have successfully created two programs of Dual PhD Degree between KAUST and, respectively, the Chinese University of Hong Kong in Shenzhen (China) and Politecnico di Milano (Italy). Several other programs both at MS and PhD are in preparation, including a joint Master with Tsinghua, University (China)and a Dual PhD Degree with Politecnico di Torino.
   b. ***Faculty and Staff Management***: I am responsible for the recruitment, retention, and professional development of faculty and staff within CEMSE. This includes all faculty hiring decisions, and evaluating faculty performance. Overall CEMSE has 69 faculty (about 14% female) and is the largest among the three divisions at KAUST. CEMSE is supported by 43 administrative and technical staff members (about 70% female), among which 27 are permanent.

[1] This included Artificial Intelligence to Computer Graphics, Networking, Cybersecurity, Computer Architectures, High Performance Computing, as well as Optoelectronics, Sensory Systems, Heterogeneous Integration, Smart Antennas, IoT Devices, Power Systems, Energy Conversion Device and Material, Advanced Semiconductors, Telecommunications and Information Science, to Methods for Advanced Numerical simulations, and Geospatial Statistics to name a few.

Faculty hiring is managed in collaboration with the *Associate Dean for Faculty* and I also coordinate the activity of the Chairs of the hiring committees, usually one per Program, plus any ad-hoc ones for areas considered of strategic interest, such as Artificial Intelligence or Cybersecurity. I am also an ex-officio member of the:

1) Promotions and Appointment Committee (PAC) – composed by the Deans of the three Divisions at KAUST, the Vice President for Research (VPR), three members at large from the Faculty body, and chaired by the Provost. The PAC makes the final recommendations to the president with respect to faculty hiring and promotion (similar to an Institute-level retention, promotion and tenure committee in many US institutions);
2) Science and Engineering Review Committee (SERC) – composed by the Deans of each Division, the Vice President for Research, and three member at large from the Faculty body, chaired by the Associate Vice President for Research. The SERC makes recommendations to the VPR for (internal) promotion to the role of Senior Research Scientist/Engineer.

MAIN RESULTS.

1) Under my leadership, **the number of faculty working in the division increased by 11% (7 FTE)**, growing specifically in the areas of Artificial Intelligence and Machine Learning (3 FTE) and Semiconductors (2 FTE);
2) I have been able to **successfully address all retention cases** (4 faculty in 3 different Programs);
3) I was involved in a very complicate cases of research misconduct, and in another less complicated cases of personal misconduct. While the each case were referred for review and ultimately dealt with appropriately with, I was also able to provide much needed protection against retaliation to the whistle-blowers, and transfer several students and post-doctoral researchers to different supervisors without any disruption in funding, research projects and, most importantly, to the student/post-doc careers;
4) I was able to successfully solve 4 "two-body" opportunities for my Division's faculty, by leveraging opportunities created in several of the structures available on campus[2];
5) I transferred the entirety of the faculty support staff's activities (procurement, business travel, business assistance,…) to a ticket-based system. This has enabled us to start measure the workload for each staff member and redistribute the load of each of them as needed, ultimately providing a uniform quality of the service provided to faculty;
6) During my tenure at KAUST, CEMSE faculty and scientists have received a significant number of individual awards and recognitions. These include:
    a) *Individual Awards by International Organizations*: the Arab Researchers Award in the Agriculture and Technology (Tareq Al-Naffouri, ECE) and the Letten Award (Paola Moraga, AMCS);
    b) *Membership of Scientific Academies:* the European Academy of Sciences Fellowship (Athanasios Tzavaras, AMCS), and the Academia Europea Membership (Roberto Di Pietro, CS; Peter Markowich AMCS; Jinchao Xu, AMCS);
    c) *Individual Awards by Professional Societies:* the Abdel El-Sharaawi Early Investigator Award, (Raphael Huser, STAT), the IEEE ComSoc Young Researcher Award (Abdelkadir Celik, ECE), the Abdul Hameed Shoman Foundation The Royal Statistical Society (RSS) Barnett Award (Marc Genton, STAT), and the Siggraph Computer Graphics Achievement Award (Wolfgang Heidrich, CS);
    d) *Fellowship in Professional Societies:* IOP (Peter Markowich, AMCS), and IEEE (Boon Ooi, ECE; Atif Shamim, ECE; Husam Alshareef, ECE).

    While I cannot certainly claim any credit for the success career of most of these researchers, I am particularly proud of the Letten Award and the elevation to IEEE Fellow, given my direct involvement in the nomination and case preparation phase.

c. ***Research Oversight***. CEMSE is involved in cutting-edge research across a range of scientific and engineering disciplines. As CEMSE's Dean I have strived to cultivate a vibrant research environment, providing support and direction in securing research funding for a wider group of faculty, and promoting collaboration within my Division and with other Divisions' faculty and staff researchers. With the launch of the Research Development and Innovation Authority (RDIA) in Saudi (equivalent to the US NSF) I have created the position of *Associate Dean for Research* to facilitate collaborative research activities among faculty and to provide support in increasing the number and quality of research projects submitted for funding to RDIA and other financial entities in the Kingdom of Saudi Arabia.

[2] KAUST campus is actually a "small village" of about 9000 people, including all supporting facilities (including K-12 school and medical systems, social outlets, etc.)

Due to my role, I am also member of the Academic Space and Equipment Planning (ASEPC) committee. ASEPC has an allocated budget of approximately $35M/year and evaluates all internal proposals by faculty for acquisition of equipment, allocates research space allotments and renovations.

The total research budget my Division is about $90M for FY2023, composed of ~$41.5M of endowed research funding for individual professors, and ~$48.5M appropriation through successful submission of proposals to competitive internal KAUST calls (73%) or sponsored by external private and public entities (27%).

MAIN RESULTS.

1) Creation of the position of the Associate Dean for Research, that has already been proven very effective given the results presented below;
2) In collaboration with the AD for Research, we were able to stimulate, support team building, and, ultimately, submit 4 expression of interest (EoI, similar to Letters of Intent and Preliminary Proposals) for creation of KAUST Centres of Excellence (CoE), namely in Cyber Secure and Resilient Systems, Semiconductors, Future Cities, and Generative AI, each to be potentially founded at $2.5M/year for 5 years. All CESME EoIs have been evaluated positively and the corresponding full proposal are currently in preparation;
3) Together with the AD for Research, we successfully stimulated the submission of average 1.25 research proposals per faculty to the first ever RDIA call. Considering that KAUST limited each faculty member to a maximum of one submission as PI per specific call, the fact that 87 proposal were submitted by faculty in CEMSE in little over two months from the publication of the call to the submission deadline was an outstanding achievement;
4) I have been able to enhance the relationship between the CEMSE Division and Aramco. Historically, Saudi Aramco has been funding research activity at KAUST, but mainly in the areas of combustion engines, energy, chemical engineering, and chemistry. I succeeded to channel their growing interest in the digital transformation of their activities, making it a steady partner of CEMSE in the areas of AI, Industrial IoT, and infrastructure monitoring.

d. ***Budget Management***: I am in charge, in partnership with the Division's Business Manager, of the Division's budget, allocating resources to support academic programs, research activities, and other divisional needs, and ensure fiscal responsibility and transparency in financial matters.

MAIN RESULTS.

1) I stimulated the creation of an online dashboard for each individual PI to increase self-awareness and self-efficacy, and improve transparency of the financial processes.

e. ***Student Affairs.*** The CEMSE student population is composed of 551 (graduate) student: 111 pursuing an MS and 439 a PhD degree. My goal is to enhance all aspects of their education within CEMSE. This includes addressing student concerns, promoting student engagement, and working to create an overall inclusive student experience as part of their educational process. Due to my role, I am also a member of the:

1) Admission Standing Committee (ASC), in charge of the final decisions on controversial student admission cases;
2) Academic Performance Committee (APC), in charge of the appeal process in student dismissal cases.

MAIN RESULTS.

1) I started a complete re-examination of the syllabus, the expected learning outcomes, and the modality of the evaluation (midterms/final exams) for all coursework offered by CEMSE, so that these aspects were as uniform as possible. This effort was to provide the students with a better learning experience and more open selection of coursework and personal program of study, and ensure a more fair distribution of workload for the faculty offering the courses.

f. ***External Relations***. I represent the Division to external stakeholders, including industry partners, government agencies, and the broader academic community. Building and maintaining strong partnerships and collaborations is an essential aspect of my role.

MAIN RESULTS.

1) I have been part of the working group, led by the KAUST President, that created the **KAUST Hub In Shenzen**. This Hub is conceived to be a vehicle for enhancing research commercialization at KAUST and in Saudi Arabia. It is also seen as a gateway for Shenzhen private and academic partners into KAUST and the KSA, and vice versa, while enabling academic collaborations between KSA and China in the area. The implementation of the MS TIE is a first important step in this direction;
2) I have been able to establish and tighten **relationship with the Saudi Ministry of Interior** (trough the development of the MPS programs on AI and Cybersecurity) and to **strengthen the relationship with Aramco** (agreement to deliver yearly the MS program on Data Science for

their employee; develop a steady partnership with CEMSE in the area of AI, Industrial IoT, infrastructure monitoring).

2. **Member Steering Board (Nucleo di Valutazione),** Politecnico di Milano, 2023 – Present. I am a member of the board, whose task is to provide critical opinion on all aspect of the activity of Politecnico. In particular, I am in charge of supervising all activity related to research quality evaluation.
3. **Rector's Delegate for Research Quality Evaluation,** Politecnico di Torino, 2019 – Present. In this role I have developed a framework enabling benchmark comparisons of the research productivity and impact of the faculty of the Politecnico di Torino with respect to Italian scientists in the same area and have been responsible for a (one year long) process of selecting the best publications of the entire University in preparation of the most recent Italian Research Evaluation Exercise (VQR2015-2019) – see also below. Such an activity has involved the coordination of a team of 5 Staff members, the training of a team of 11 faculty colleagues, one per department, and supervision of the entire selection process.
   I am also in charge of the methodology for using publications outputs to determine which are the scientific areas where Politecnico di Torino should expand. This activity involves a coordination with the Academic Senate and the Board of Directors of the Politecnico. I continue to work in this role remotely.
4. **Associate Department Chair for Research**, Department of Electronics and Telecommunications (DET), Politecnico di Torino, 2019–2022. The role of the committee is to propose strategic research directions for the Department and to promote research collaborations. One of my main activities has been to mentor early career colleagues in writing research projects, both at National and EU level, and to promote the cooperation between department colleagues of different areas. Most recently, the focus has been to guarantee their involvement in the various project in the framework of the EU Resilience and Recovery Plan (PNRR), the European initiative to guide the economy and society out of the recession due to the Covid-19 pandemic.
   More specifically, at the Department level, I am involved in the PNRR's creation of the "competence centers" (specifically, in the areas of "Smart Mobility", which includes electric traction and power conversions for automotive, autonomous driving …, and "High Performance Computing" which includes the development of innovative CPU/GPU platforms for Big Data processing to Quantum Architectures) and "extended partnerships" (in the area of Artificial Intelligence, Aerospace, Future of Telecommunications, Smart Medical Systems, Cybersecurity…). The budget available for the formation of the corresponding consortia of Italian Universities/Industries is about €3.2 billion
5. **Member**, 2018-now, Supervising Board, Ph.D. program on Electrical, Electronic and Communications Engineering, Department of Electronics and Telecommunications (DET), Politecnico di Torino.
6. **Co-proposer**, 2016, Master Program on Advanced Automotive Electronic Engineering. This is part of the MUNER (Motorvehicle University of Emilia-Romagna), which is a joint effort of all Universities of the Emilia Romagna Region (Bologna, Modena, Ferrara and Parma) to develop highly specialized course on all aspect of advanced car manufacturing in cooperation with some of the most important car manufacturers like Lamborghini, Dallara, Ducati, Ferrari, and Maserati, in additions to several others companies located in the so-called Motor Valley. I personally worked with other two colleagues to set up the curricula for the first edition of the program which took place in 2017-2018.
7. **Chair, Group of Experts for Evaluation (GEV)**, 2015-2017, for the area of Information and Industrial Engineering (GEV09), of the Evaluation of Research Quality Exercise 2011-2014 (VQR2011-2014).

   The VQR is one of the biggest evaluation initiatives ever carried out worldwide, realized with the objective to give a detailed picture of the quality of higher education and research in Italy. It is coordinated by ANVUR, the National Agency for the Evaluation of the University and Research Systems, which nominated the GEVs, one for each area of both sciences and human sciences. The first edition, VQR2004-2010 analyzed the quality of research of 133 research bodies in 14 areas: 95 universities, 12 public research bodies under the vigilance of the Italian Ministry of Education, University and Research (MIUR) and 26 additional organizations (9 research bodies and 17 inter-university consortia). For the VQR2011-2014, I was also the chair of the working group in charge of computing, for every journal paper, a normalized bibliometric information to make its impact easily comparable with all other papers in the same area. Furthermore, GEV09 under my leadership was responsible to assess the impact of more than 12000 products, using both peer review, the above mentioned normalized bibliometric information of impact, and the assessment of 40 GEV members. My consensus building skills have been important in this case to ensure that all members were in agreement with the guidelines to assess the product impact and to make sure that all evaluation criteria were uniformly applied by all GEV members, so as to guarantee a fair evaluation for every product.
2. **Member, Group of Experts for Evaluation (GEV),** 2011-2013, for the area of Information and Industrial Engineering, of the Evaluation of Research Quality Exercise 2004-2010 (VQR2004-2010). The group has been given the task to oversee the classification process of the research products of Italian universities and research centres, by means of peer review and using bibliometric indicators.

3. **Associate Department Chair for Internationalization and Students Mobility,** 2011-2016, Department of Engineering, University of Ferrara. I was in charge of managing existing cooperation relationships between the Department and foreign universities/research institutions and to promote creation of new international relationships.
4. **Chair**, 2010-2011, Evaluating Committee for the Faculty of Engineering, University of Ferrara Strategic Research Projects.
5. **Coordinator of the Project**, 2002-2010, European Ph.D. Program on Information Technology (EDITH), Advanced Research Center on Electronic Systems for Communication and Information Technology (ARCES), University of Bologna. I prepared the proposal to the European Community and administered the EDITH project after it was funded with approximately 2M€ following an extremely competitive selection in which only 7% of 750 proposals were funded. The European Ph.D. program partners included:
   a) DIMES, Delft University of Technology, The Netherlands;
   b) EPFL-I&C, I & C School, Swiss Federal Institute of Technology, Lausanne, Switzerland;
   c) IMEP, Institut National Polytechnique de Grenoble, France;
   d) SCD-K.U.Leuven, EE Dept. (ESAT), Faculty of Engineering (FTW), Katholieke Universiteit Leuven;
   e) CEA-LETI, Commissariat à l'Energie Atomique, Laboratoire d'Electronique, de Technologie de l'Information, France;
   f) IMEC, Interuniversitair Micro-Elektronica Centrum, Belgium.

   In this framework, **I was able to establish agreements** between University of Bologna and K.U. Leuven, INPG, IMEC and CEA-LETI **to award a double Ph.D. title to students performing their work in any two Institutions within the partnership project**.
6. **Area Coordinator** 2005-2013, Area of Circuits, systems and algorithms for signal processing (A6), Advanced Research Center on Electronics Systems for Information and Communication Technologies (ARCES), University of Bologna. ARCES was established in 2001 after approval by the Ministry of Education, University and Research (MIUR) as an initiative to set up a Center of Excellence (EC) in the area of Information and Communication Technology (ICT). ARCES involves 38 faculty and has the mission of promoting and facilitating interdisciplinary research in all areas of ICT, exploiting the scientific competences of its members in the fields of Semiconductor Device Physics, Integrated Circuit Design, Signal Processing and Algorithms, Non-Linear Control, Communications Techniques and Systems, Bio-Electronics, Geomatics, Navigation Systems Control, Computer Vision, and Applied Mathematics and Geometry. The main research areas were:
   A1 CMOS sensors and signal-processing architectures
   A2 Computer vision and image-processing systems
   A3 Advanced wireless communication systems
   A4 Satellite systems for navigation control and real-time kinematic
   A5 Device simulation and quantum computing
   A6 Circuits, systems and algorithms for signal processing

   I have been responsible for Area 6 since 2005, and in this role, which made me a member of the I was responsible for Area 6 since 2005, and a member of the Executive Committee of ARCES. In this role I was able to provide leadership that allowed the Center to flourish despite the organizational difficulties created by its unconventional non-departmental structure, particularly in the interactions/relationships with the Electronic and Computer Engineering Department of the University of Bologna. ARCES indeed achieved a number of important results consolidating its structure, strengthening its research organization, and gaining a wider recognition both locally and within the scientific community at large. ARCES also proved its ability to devise new projects at the forefront of advanced research in ICT (for some of which I acted as PI/Co-PI), and to secure the financial resources needed to ensure its growth and success. As an example, one of the most important factors enabling the success of ARCES was the creation of a PhD program in ICT (the EDITH program mentioned above). This PhD program was designed and administered with a focus on international partnerships, a significant departure from the PhD programs offered by academic departments at the University of Bologna. The existence of these differences was one of the key reasons why the program was able to attract students with excellent scientific skills.
7. **Coordinator**, 2005-2011, MIUR Internationalization project ACASTI, University of Ferrara. Project partners included:
   a) Queen Mary University of London, UK;

b) Swiss Federal Institute of Technology in Lausanne (EPFL), CH;
c) IBM, T. J. Watson Research Laboratories, US;
d) University of California San Diego (UCSD), US;
e) Northeastern University, Boston, US;
f) STMicroelectronics, Wireless Research Center, Geneva, CH;
g) University of Washington, US;
h) Katholieke Universiteit Leuven, BE.

7. **Member**, 2002-2005, 2008-2012, Executive Committee, Department of Engineering, University of Ferrara.
8. **Member**, 1998-2003, 2012-2017, Supervising Board, Ph.D. program on Information Technology, Department of Engineering, University of Ferrara.

4. Professional Activities

4.1 PRINCIPAL ACTIVITIES FOR IEEE

4.1.1 *Leadership/Management*

Leadership positions are reported in decreasing order of perceived importance and in reverse chronological order. Whenever deemed important a short explanation of the impact of the service I performed is also provided.

1. **IEEE Vice President for Publication Services and Products**, (VP-PSP) 2013 and 2014 (two consecutive elected terms). This was **the first time in the history of IEEE** in which **a Scientist not from North America** had been elected to this role.
   The VP-PSP is responsible for providing leadership in the strategy for producing and delivering IEEE's information services and products; for providing oversight for policies ensuring the editorial integrity, quality, and competitiveness of IEEE's intellectual property and its protection; and for ensuring the financial health of IEEE's Publishing Operations. For example, the VP-PSP is responsible for taking decisions of affecting all IEEE and the wider scientific community, such as for improving IEEE Xplore functionalities, for managing the IEEE Publication portfolio to be able to capture the most important new technological trends and developments, and for making sure that the vetting process (peer review) for all information published by IEEE is both timely and adherent to the highest standards of quality. Furthermore, together with the Treasurer of the PSP board, the VP-PSP is responsible to ensure that the financial operations of IEEE publications are sound and aligned with the objectives of IEEE and in doing so, manages a budget in excess of $150M. The VP-PSP chairs a board of approximately 30 volunteers from industry, research laboratories, and academia, and coordinates with a group of more than 20 senior IEEE staff led by the IEEE Staff Executive for Publication, who reports directly to the IEEE Executive Director.
   Among my accomplishments in this role, has been raising awareness within IEEE of the weakness of journal bibliometric indicators (specifically, Impact Factor) and their increasingly frequent misuse in assessing individual scientists' performance for hiring, tenure and promotion, or for research proposal evaluation. More concretely, I was:
   a) able to promote, within IEEE, the adoption of multiple and more reliable journal metrics, such as the EigenFactor and the Article Influence, for assessing the impact of a periodical and to highlight the needs of assessing the impact of individual papers through article level metrics. Concrete outcome of this activity are display of three different journal metrics on each journal home page in IEEE Xplore – as an indication that IEEE does not favour any of those in particular – and display of individual article citations, downloads, and paper views for each published paper on IEEE Xplore – to highlight that an *article's* impact cannot be measured using the *journal*'s metrics as proxies;
   b) successful in obtaining the approval by the IEEE Board of Directors in September 2013 of the IEEE Statement on Correct Use of Bibliometric Indicators (for more information http://www.ieee.org/publications_standards/publications/rights/bibliometrics_statement.html). This was a first and fundamental step to provide leadership in fighting bibliometrics misuse and, hence, in having a concrete positive impact in the way scientific activity is evaluated for many members of the IEEE community. Since 2013, I have launched a significant initiative to educate the community on this important matter by presenting overviews at major IEEE conferences (including CDC, ISCAS, and PES General Meeting), at the US **National Science Foundation,** and at the 2015 Electrical and Computer Engineering Department Heads Association meeting. Currently this educational effort is being institutionalized within IEEE with the preparation of handout material to each Editor-in-Chief of an IEEE journal as part of their onboarding process[3]..
2. **Member, IEEE Board of Directors (BoD)**, 2013-2014. The BoD is the highest governing body of the IEEE and has the legal responsibly to oversee the management of the IEEE and serve the best interests of the Institute, its members and the public. This was an important experience which exposed me to the practices and regulations which are typical in the administration of a large legal entity (non-profit in particular). As a BoD member I had to oversee the IEEE's current business (USD $450 Million operating budget) and financial performance, future business prospects and forecasts, financial statements with appropriate segment or divisional breakdowns, compliance programs with applicable law and corporate policies, material litigation, governmental and regulatory matters, and monitoring and, where appropriate, responding to communications from members.
   As examples of my achievements in this role, I was instrumental in the preparation of responses to requests for comments on proposed Open Access mandates by funding agencies and inquiries on bibliometrics manipulation, and was involved in decisions related to legal disputes involving manuscripts

[3] See for instance https://ieee.webex.com/ieee/lsr.php?RCID=f617e2f3552086d028cfdf52e189a2c7

suspect of plagiarism, as well as in the process of determining performance salary incentives for high-level IEEE staff members..

3. **President**, **IEEE Circuits and Systems Society**, (CASS) 2010 (President-elect in 2009, Past-President in 2011). This was the first time in the history of CASS that a scientist of an Italian institution was elected in this position. In this role I succeeded in:
   a. creating two new publications sponsored by the CAS Society, namely the IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) and the IEEE Virtual Journal on Radio Frequency Integrated Circuits (RFIC VJ);
   b. reducing workload for conference technical committees for International Symposium on Circuits and Systems (ISCAS) through a mid-term contract and commitment to a single paper selection platform and software. This resulted in improved decision making process and improved authors/reviewers satisfaction in the subsequent years;
   c. increasing the effective value of CAS Membership, by providing free on-line access to JETCAS and to RFIC VJ, and offering free on-line access to all CAS sponsored publications and conference proceedings to CAS *student* members;
   d. improved the impact of the President's role by extending the mandate to 2 years from a previous 1-year long role;
   e. improved agile decision making at the highest leadership level within the Society, i.e., the CAS Executive Committee (ExCom), by reducing the number of ExCom members;
   f. enhancing abiity to make an impact on regional activities, by increasing involvement of a larger number of BoG members in membership activities.
4. **Chair**, **IEEE TAB Transactions Committee**, 2018-2020. The committee is composed by the EiC of all IEEE Transactions and Journals and has the function of deliberating on, as well as coordinating and harmonizing policies related to IEEE journals. I was the **first Italian** to occupy this position in the history of the IEEE.
5. **Chair,** 2012 and **Member**, 2011 and 2013-2022**, PSPB Strategic Planning Committee**. In this role, I succeeded in raising awareness within IEEE of the weakness of Impact Factor as a quality measure for journal publication and in promoting the use of EigenFactor and Article Influence as more reliable and complementary alternatives.
6. **Chair, IEEE Board of Directors Ad Hoc Committee on the Future of Information & Convening,** 2015. This committee had the charter to examine possible scenarios pertaining to the way in which information will be produced, made available and consumed over five-, ten- and fifteen-year periods, and which actions IEEE should undertake immediately to anticipate and address those activities. The most important outcome of this activity was to **provide leadership within IEEE in promoting and developing a culture of reproducibility in research** (that is, the possibility for independent parties to reproduce the scientific results presented in a published paper).
   I strongly believe that the topic of research reproducibility (RR) will continue to grow in importance over the coming years. Since my efforts at IEEE in 2015, there has been an increasing interest of funding agencies in RR: in the US and around the World, governmental agencies are requiring (for results obtained in the framework of their funded projects), not only accessibility of the resulting outcomes through archiving in open-access repositories, but also data management plans (including metadata, algorithms, codes etc.). Such efforts are fueled not only by the need to strongly advertised the outcomes of the research produced through use of public funds, but also (and perhaps more importantly) due to the continued "discovery" of replication of published work even in prestigious publications; the most publicized examples of such "research waste" are in Life Sciences, but **similar cases are becoming more common also in the areas of Physics and Engineering**. **This diminishes the (perceived) value of research** resulting in an effective and significant financial loss, for research supported by public funds.
   Examples of concrete actions related to my leadership in RR are:
   a. participation as a panellist at the workshop on "Statistical Challenges in Assessing and Fostering the Reproducibility of Scientific Results" held at the **US National Academy of Sciences** in February 2015, to share IEEE experiences on first attempts towards RR.
   b. Contributed to the writing and preparation of an NSF Grant 1641014 "Research Communication 2020 - Proposal to fund a workshop on data and software curation and the relationship to reproducible research" led by another member of the IEEE Board of Directors Ad Hoc Committee on the Future of Information & Convening, Prof. John Ballieul (Boston University). Subsequent to funding, I was a member of the steering committee of the workshop which was held in Washington DC on November 5-6, 2016 (for further details see

http://www.ieee.org/publications_standards/publications/ieee_workshops/research_reproducibility.html and https://www.nsf.gov/awardsearch/showAward?AWD_ID=1641014).

c. participation as a panelist at the NAS meeting on "Reproducibility and Replicability in Science Meeting" held at the **US National Academy of Sciences** in February 2018, contributing to the stakeholders data gathering central in establishing of best practices in RR (see http://sites.nationalacademies.org/sites/reproducibility-in-science/index.htm).

d. Reviewer of the report of the NAS committee on Reproducibility and Replicability in Science. The report was issued in May 2019 (see https://www.nap.edu/catalog/25303/reproducibility-and-replicability-in-science)

7. **Member**, IEEE Fellow Committee, 2018-2020, 2023-2024. The IEEE Fellow Committee has the ultimate responsibility to elect IEEE Fellows each year after a process which is about 6 months long, involving evaluation of approximately 100 Fellow nomination forms by each of the 50 members of the committee.
8. **Member**, IEEE Fellow Strategic Planning Committee, 2018-2020. In this role, I was instrumental to streamline the evaluation process of the Fellow selections improving its fairness.
9. **Member**, IEEE Governance Committee, 2015, 2018-2020 (GOV). The GOV committee is responsible for reviewing, on a regular basis, the overall corporate governance of the IEEE, evaluating overall governance effectiveness and efficiency; recommending improvements with respect to need, appropriateness and effectiveness, e.g., improvements to the Board's operations, and to the IEEE Bylaws, Policies, or related documents. In this role, I had the opportunity to become familiar with the structure of bylaws and policies of a high level of complexity.
10. **Member**, IEEE Nominations and Appointments Committee, 2015, 2016 (N&A). The IEEE N&A Committee is responsible for making recommendations of the most qualified individuals for positions elected by the IEEE Assembly and appointed or recommended by the IEEE Board of Directors. This includes, for instance, the members of the IEEE Fellow Committee, the IEEE Awards Board, and the possible candidates for the role of IEEE President. In this role, I had the opportunity to enhance my ability to identify key talents for a specific position.
11. **Member**, IEEE Board of Directors Strategic Planning Committee, 2013. The committee has the role to discuss and define the main strategies for the entire IEEE. In this role I helped to define the IEEE priorities at that time.
12. **Member**, IEEE Board of Directors Ad Hoc Committee on Engagement in Europe, 2013-2015. The Ad Hoc Committee on Engagement in Europe worked to expand IEEE's engagement with, and support of, the European engineering community, which included at the time nearly 60,000 IEEE members. The committee is now a permanent committee of the IEEE BoD.
13. **Member**, IEEE Board of Directors Ad Hoc Committee on Information Technology, 2014. The committee had the charter to rationalize the activity of IT management and product development within IEEE.
14. **Member**, IEEE Periodicals Review and Advisory Committee (PRAC), 2011-2012, 2018-2019. The committee has the responsibility to conduct peer review evaluation of all aspects and facets of the publication related to periodicals published by IEEE to ensure that they meet its rigorous publication standards.
15. **Member** IEEE TAB Periodical Committee (TAB-PC), 2011-2012, 2018-2020. The committee has the role to approve the proposal for new IEEE publications and revise their scope.
16. **Member** IEEE Publication Services and Products Board (PSPB), 2011-2012, 2015-2022. The committee has the responsibility of overseeing all publications of the IEEE ranging from journals to conferences and including products such as IEEE Xplore.
17. **Vice-Chair,** 2016-2017 and **Member**, 2011, IEEE Circuits and Systems Society Fellow Committee
18. **Member, Board of Governors (BOG)**, IEEE Circuits and Systems Society, 2005-2007. Re-elected for a second term 2008-2010.
19. **Chair, Long-Term Strategy Planning Committee**, IEEE Circuits and Systems Society, 2006. In this role, I was instrumental in the creation of the *CAS Society Newsletters* and in the establishment of criteria to improve quality and impact of the International Symposium on Circuits and Systems (ISCAS).
20. **Member, Long-Term Strategy Planning Committee**, IEEE Circuits and Systems Society, 2005, 2007, 2008.

4.1.2 Journals (Editorship/Guest-Editorship)

Roles are reported in order of importance from Editor-in-chief (EIC) to Editor/Associate Editor, to Guest Editor. For each category order is reverse chronological.

1. **Editor-in-Chief,** PROCEEDINGS OF THE IEEE, 2019-2024 (reappointed for a second 3-year term in 2022). The Proceedings of the IEEE **is the Flagship publications of the IEEE** (2020 IF = 10.961 (Clarivate),

2020 CitesScore = 21.6 (Scopus)) and provides in-depth review, survey, and tutorial coverage of the technical developments in electronics, electrical and computer engineering, and computer science. Consistently ranked as one of the top engineering journals by Impact Factor, Article Influence Score, and CiteScore, the journal serves as a trusted resource for engineers around the world. The editorial board is composed only by IEEE Fellows. **I am the first non-US scientist** to be selected by the IEEE PSPB for the role of EiC in the history of the journal, which can be traced back to its early beginnings in 1909 (when it was known as the Proceedings of the Wireless Institute).

2. **Editor-in-Chief**, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I, 2008-2009. I was the second Italian scientist to serve as TCAS-I EiC and the youngest EiC in the history of the journal dating back to the its establishment in 1960 as the IEEE Transactions on Circuit Theory. In this role, I reduced the average first decision time to about 68 days and the average submission-to-electronic publication to 8 months, reducing it by around 40%. This had no adverse impact on the quality of the journal: in fact, a) the acceptance rate decreased to about 21% and b) the two "per-article" bibliometric indicators published by Clarivate, i.e. the Impact Factor and the Article Influence Score, in 2008 increased to 2.042 and 0.870, the highest TCAS-I had since its inception.

   I also strengthened the collaboration with journals of "sister" societies, with particular emphasis to the Journal of Solid State Circuits, with which TCAS-I has now a yearly joint special section as a follow-up of the CICC conference.

3. **Editor-in-Chief**, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-II, 2006-2007. I was the first Italian scientist to serve as TCAS-II EiC as well as the youngest one. In this role I succeeded in reducing the average first decision time to less than 60 days and the average submission-to-publication time to less than 7 months, without impacting the journal quality. The only bibliometric measure available from Clarivate until that point, namely the journal Impact Factor, increased to 1.012 in 2007, which was the highest for TCAS-II since its inception. I also introduced a highly improved version of the web review system interface for all CAS Society journals, which proved instrumental in achieving the above mentioned results.

4. **Deputy Editor-in-Chief**, IEEE CIRCUITS AND SYSTEMS MAGAZINE, 2004-2007. In this role, I introduced thematic special issues starting in 2006. This approach proved to be a key strategy in attracting a strong interest in the publication, as proven by the fact that the 2009 5-years-IF of the CAS Magazine was as large as 7.54, the highest that year among all publications in the entire area of Electrical and Electronic Engineering.

5. **Associate Editor,** PROCEEDINGS OF THE IEEE, 2015-2018.

6. **Editorial Board Member,** IEEE Spectrum, 2018

7. **Editor**, IEEE ACCESS, 2013-2015.

8. **Associate Editor**, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-II, 2004-2005, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I, 1999-2004.

9. **Guest-Editor** of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS – PART I, Special Issue on "ISCAS 2015", May 2016.

10. **Guest-Editor** of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS – PART I, Special Issue on "ISCAS 2014", May 2015.

11. **Guest-Editor** of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, Special issue on "BioCAS 2013", October 2014.

12. **Guest-Editor** of the IEEE JOURNAL ON SELECTED AND EMERGING TOPICS IN CIRCUITS AND SYSTEMS, Special issue on "Circuits, Systems and Algorithms for Compressive Sensing", September 2012.

13. **Guest-Editor** of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS – PART I, Special Issue on "ISCAS 2008", May 2009.

14. **Principal Guest-Editor**, PROCEEDINGS OF THE IEEE, Special issue on "Applications of Nonlinear Dynamics to Electronic and Information Engineering", May 2002.

4.1.3 Conferences

The different roles that I had in scientific/organizing committees for international conferences are reported below. They are listed in decreasing order of importance (from General Chair to Technical Program Chair to arrive to member of the Technical Program Committee) and in reverse chronological order.

1. **Co-Chair, General,** *IEEE International Symposium on Circuits and Systems (ISCAS2018), Florence, Italy*, 2018. This was the **second time in the history** of the conference (which dates back to 1968) that ISCAS was organized in Italy (the first one was in the early 80's and was chaired by Prof. Antonio Ruberti, former Minister of Education in Italy). In this role, I was instrumental to steer ISCAS technical

program towards innovation themes like *Internet of Things, Cognitive Computing and Deep Learning, Big Data Processing, Industry 4.0, Smart Systems for Automotive, Personalized Healthcare Systems, and EDA Methodologies*. I also introduced innovation in the conference structure to be able publish the conference proceedings, Open Access for 3 weeks, in IEEE Xplore **before the conference** (Open Preview), and to publish a select set of the highest quality papers directly in the IEEE Transactions on Circuits and Systems Part – II before the conference. I was responsible for preparing the bid for the conference and succeeded in obtaining it against 8 other candidate venues and organizing teams.

2. **Co-Chair, General,** *IEEE/IEICE International Symposium on Nonlinear Theory and its Applications (NOLTA2006)*, Bologna, Italy, 2006.
3. **Chair, General**, *Nonlinear Dynamics and Complexity in Information and Communication Technology (NDICT2004)* (now IEEE International Conference on Complex Systems and Networks, IWCSN), Bologna, Italy, 2004.
4. **Co-Chair, Technical Program**, *IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS2024)*, Abu Dhabi, UAE, 2024.
5. **Co-Chair, Technical Program**, *IEEE Midwest Symposium on Circuits and Systems (MWCAS2023)*, Phoenix, USA, 2023.
6. **Co-Chair, Technical Program**, *IEEE Biomedical Circuits and Systems Conference (BioCAS2013)*, Rotterdam, The Netherlands, 2013.
7. **Co-Chair, Technical Program,** *IEEE International Conference on Electronics, Circuits, and Systems (ICECS2012)*, Seville, Spain, 2012.
8. **Co-Chair, Technical Program,** *IEEE International Symposium on Circuits and Systems (ISCAS 2008)*, Seattle, USA, 2008. In this role for ISCAS2007 and ISCAS2008 I was instrumental in assuring a continuation in the trend of improvement of the technical quality of the conference, which resulted in an acceptance rate of about 43% over approximately 2000 submissions.
9. **Co-Chair, Technical Program,** *IEEE International Symposium on Circuits and Systems (ISCAS 2007)*, New Orleans, USA, 2007.
10. **Co-Chair, Technical Program**, *IEEE International Special Workshop on Nonlinear Dynamics of Electronics Systems (NDES2000)*, Catania, Italy.
11. **Co-Chair, Special Sessions**, *IEEE International Symposium on Circuits and Systems (ISCAS 2006)*, Kos, Greece. In this role for ISCAS2005 and ISCAS2006 I created a new procedure for selecting Special Session proposals which resulted in an improvement of the technical quality of the selected sessions and which is still adopted for ISCAS.
12. **Co-Chair, Special Sessions,** *IEEE International Symposium on Circuits and Systems (ISCAS 2005)*, Kobe, Japan, 2005.
13. **Chair, Track** on Nonlinear Circuits and Systems at the *IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2011)*, Beirut, Lebanon.
14. **Chair, Track** on Nonlinear Circuits and Systems at the *IEEE International Symposium on Circuits and Systems (ISCAS 2004)*, Vancouver, Canada.
15. **Member of the Technical Program Committees**:
    a) *IEEE International Symposium on Circuits and Systems (ISCAS)*: 2000, Geneva, Switzerland; 2001, Sydney, Australia; 2003, Bangkok, Thailand; 2004, Vancouver, Canada; 2005, Kobe, Japan; 2006, Kos, Greece; 2007, New Orleans, USA; 2008, Seattle, USA; 2009, Taipei, Taiwan; 2010, Paris, France; 2011, Rio de Janeiro, Brazil; 2012, Seoul, Korea; 2013 Beijing, China; 2014 Melbourne, Australia; 2015 Lisbon, 2016 Montreal, Canada; 2017 Baltimore, USA; 2019 Sapporo, Japan; 2020 Seville, Spain; 2021 Daegu, Korea; 2022 Austin, USA, 2023 Monterey, USA
    b) *IEEE Asia Pacific Conference on Circuits and Systems (APCAS)*: 2008, Macao, China
    c) *IEEE International Specialists Workshop on Nonlinear Dynamics of Electronics Systems (NDES)*: 2000, Catania, Italy; 2001, Delft, The Netherlands; 2002, Izmir, Turkey; 2003, Scuol, Switzerland; 2004, Evora, Portugal
    d) *IEEE/IEICE International Symposium on Nonlinear Theory and its Applications (NOLTA)*: 2004, Fukuoka, Japan; 2005, Bruges, Belgium; 2006, Bologna, Italy; 2007, Vancouver, Canada 2008, Budapest, Hungary; 2009, Sapporo, Japan; 2010, Krakow, Poland; 2011, Kobe, Japan; Palma de Majorca, Spain, 2012, Santa Fe, USA, 2013; Luzern, Switzerland, 2014, Hong Kong, China, 2015.
    e) *IEEE International Conference on Biomedical Circuits and Systems (BioCAS)*: 2012, Hsinchu, Taiwan; 2013, Rotterdam, The Netherlands; 2014, Lausanne, Switzerland; 2015, Atlanta, Georgia;

2016 Shanghai, Cina; 2017 Turin, Italy; 2018 Cleveland, USA; 2019 Nara, Japan; 2021 Berlin, Germany; 2022 Taipei, Taiwan; 2023 Toronto, Canada.

4.2 ACTIVITIES FOR OTHER ENTITIES

4.2.1 Journals (Editorship/Guest-Editorship)

1. **Editor**, *Nonlinear Theory and Its Applications (NOLTA), IEICE,* 2010-
2. **Associate Editor**, *Hindawi Journal of Electrical and Computer Engineering,* 2008-2021
3. **Guest-Editor** of the *IEICE Transactions on Fundamentals*, Special Section on "Multi-dimensional Mobile Information Networks", July 2006.
4. **Guest-Editor** of the *IEICE Transactions on Fundamentals*, Special Section on "Nonlinear Theory and its Applications", September 2007.
5. **Associate Guest-Editor** of the *IEICE Transactions on Fundamentals* Special Section on "Nonlinear Theory and its Applications", September 2004.
6. **Associate Guest-Editor** of the *IEICE Transactions on Fundamentals* Special Section on "Nonlinear Theory and its Applications", September 2005.
7. **Associate Guest-Editor** of the *IEICE Transactions on Fundamentals* Special Section on "Nonlinear Theory and its Applications", September 2006.

4.2.2 Conferences

1. **Member of the Technical Program Committees**:
   a) *European Conference on Circuit Theory and Design (ECCTD)*: 2003, Krakow, Poland; 2005, Cork, Ireland; 2007, Seville, Spain; 2009, Antalya, Turkey; 2011 Linköping, Sweden; 2013, Dresden, Germany, 2015, Trondheim, Norway; 2017 Catania, Italy.
   b) *IASTED International Conference on Circuits, Signals, and Systems (CCS)*: 2007, Banff, Canada; 2008, Hawaii, USA

4.2.3 Reviewer Activity for Awards and Research Projects

1. Invited by the *National Science Foundation* (NSF), USA, to act as a reviewer of research projects in the field of *Information Technology Research (ITR)*.
2. Invited by the *Engineering and Physical Sciences Research Council* (EPSRC), UK, to participate in the college of peer review.
3. Invited by the *Science Foundation Ireland* (SFI), IR, to act as a reviewer of their Investigator programmes.
4. Invited by the *National Research Foundation of the UAE* (NRF), UAE, to act as a reviewer of their Research & Scholarship Awards programmes.
5. Invited by the *Dutch Technology Foundation* (STW), NL, to act as a reviewer of their Technology oriented Sciences in the Netherlands Awards programmes.
6. Invited by the *Italian Ministry of Research and Education* (MIUR), I, to act as a reviewer of their Young Investigators Awards programmes.
7. Invited by the *Italian Piemonte Region*, to act as a reviewer of their Regional Projects Awards programme.
8. Invited by the *Cyprus Research Promotion Foundation* (RPF), CY, to act as a reviewer of their Young Researcher from Abroad Awards programme.
9. Invited by the *Science and Technology Foundation of Japan*, to act as a proposer for the 2003 Japan Prize in the field of *"Science and Technology of Complexity"* and for the 2005 Japan Prize in the field of "*Information and media technology.*" The amount of the prize is approximately 500K EURO (http://www.japanprize.jp).
10. Chair, CAS subcommittee for the IEEE Transactions on CAS – Part I and IEEE Transactions on CAS – Part II best paper awards (2006-2009).

4.3 SELECTED TUTORIALS AND INVITED TALKS

4.3.1 Plenary Lectures

1. *IEEE Biomedical Circuits and Systems Conference (BIOCAS2023)* Lecture on "Compressive Sensing for Biomedical Applications: Is this a Hammer Looking for Nails?," Toronto, Canada
2. *International Workshop On Mathematical Issues In Information Sciences (MIIS2023)* Lecture on "Techniques for TinyML: from Classical Pruning Methods to a New Neuron Paradigm for DNNs," Shenzen, China
3. *RESMIQ Innovation Days 2015 (RID2015)*, Lecture on "Compressive Sensing: From Algorithms to Circuits", Microsystems Strategic Alliance of Québec (ReSMiQ), Montreal, Canada.

4. *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS2012)* Lecture on "Compressive Sensing: From Algorithm to Circuits and Systems Architectures", Kaohsiung, Taiwan
5. *IEEE International Conference on Green Circuits and Systems (ICGCS2010),* Lecture on "EMI Reduction Methods Based on Nonlinear Dynamics," Shanghai, China.
6. *IEEE International Conference on Electronics, Circuits, and Systems (ICECS2008),* Lecture on "Information Technology Applications of Statistical Nonlinear Dynamics," Valletta, Malta.
7. *IEEE/IEICE International Symposium on Nonlinear Theory and its Applications (NOLTA2005)*, Lecture on "Information Technology Applications of Statistical Nonlinear Dynamics: Key Results and Future Trends," Bruges, Belgium.

In addition to these plenary lectures, I have also given **25 invited talks** in special sessions/workshop organized in several conferences (see full list of publications).

4.3.2 Invited Talks

I have (co-)organized several tutorial sessions (as reported in the next section) and delivered more than 70 invited seminars/talks, as well as 14 lectures in the framework of the CAS Society Distinguished Lecturers Program (which is additional evidence of my capability to deliver high impact lectures which are greatly appreciated by the audience). A selected list is reported below.

1. "Tiny Machine Learnin: from Classical Pruning Methods to a New Neural Paradigm for DNNs," Machine Learning Center at Georgia Institute of Technology (invited by Prof. Nazanin Bassiri-Gharb), Februray 2024
2. "Compressive Sensing: From Algorithms to Circuits," Department of Electrical and Systems Engineering, University of Pennsylvania (invited by Prof. Jan Van der Spiegel), September 2019.
3. "Compressive Sensing: From Algorithms to Systems Implementation," Silicon Labs, Austin, USA (invited by Dr. Alessandro Piovaccari, CTO & SVP of Engineering), August 2019.
4. Compressive Sensing: From Algorithms to Circuits," NXP Semiconductors, Eindhoven, NL (invited by Dr. Alessio Filippi, Head, Automotive Business Unit), September 2018.
5. "Compressive Sensing: From Algorithms to Circuits," Institute for Systems Research (ISR), University of Maryland, College Park, MD, USA (invited by Prof. Pamela Abshire), June 2017.
6. "Compressive Sensing: From Algorithms to Circuits," and on "Is Spread Spectrum Clocking Effective for EMI Reduction?" Department of Electrical and Electronic Engineering Technology, University of Johannesburg, South Africa (invited by Prof. Paul Babu, Head of Department), August 2016.
7. "Compressed Sensing: from Algorithm to Circuits," Department of Electrical and Computer Engineering, Tufts University, Boston (invited by Prof. Sameer Sonkusale), June 2016
8. "Compressed Sensing: from Algorithm to Circuits," Analog Devices, Boston (invited by Dr. Gabriele Manganaro), June 2016
9. "Compressed Sensing: from Algorithm to Circuits," Micro- and Nanosystems Laboratory, ETH, Zurich (invited by Prof. Cristopher Hierold), May 2016
10. "From Algorithms to Circuits: Synergetic Design and Optimization," Whiting School of Engineering, Johns Hopkins University, Baltimore, USA (invited by Prof. Ralph-Etienne Cummings), April 2016
11. "Compressive Sensing: From Algorithms to Circuits," and on "Is Spread Spectrum Clocking Effective for EMI Reduction?" Faculty of Electrical Engineering and Communication, Brno University of Technology, Brno and Faculty of Electrical Engineering, Czech Technical University in Prague (invited by Prof. Norbert Herencsar), December 2015.
12. "Compressive Sensing: From Algorithms to Circuits," Air Force Research Laboratory AFRL/RW, Eglin, FL, USA (invited by Dr. Martin Wehling), September 2015.
13. "Compressive Sensing: From Algorithms to Circuits," Department of Electronics, Universidade Federal do Rio de Janeiro (UFRJ), Rio de Janeiro, Brazil, (invited by Prof. Eduardo da Silva), June 2015.
14. "Compressed Sensing: From Algorithms to Circuits" Texas Instruments, Santa Clara, CA, USA, (invited by Dr. Chatterjee Bijoy), October 2014.
15. "Is Spread Spectrum Clocking Effective for EMI Reduction?" Texas Instruments, Santa Clara, CA, USA, (invited by Dr. Chatterjee Bijoy), October 2014.
16. "Hardware Efficient Random Numbers Generation with Chaos," (invited by Prof. Jinhu Lu, Chinese Academy of Science, Beijing) *International Workshop on Complex Systems and Networks (IWCSN2013)*, Beijing, China, September 2010.
17. "Is Statistical Nonlinear Dynamics Useful in Electronic Circuit Design?" National Semiconductors, Santa Clara, CA, USA, (invited by Dr. Chatterjee Bijoy), April 2010.

18. “High Throughput True Random Number Generation Based on Nonlinear Dynamics”, (invited by Dr. Chai Wah Wu, IBM T. J. Watson Research Laboratories, Yorktown Heights, NY), J. T. Watson Research Laboratories, Yorktown Heights, USA, August 2007.
19. “Chaos-Based Generation of Optimal Spreading Sequences for DS-UWB Sensor Networks," (invited by Prof. M. Tse, Hong Kong Polytechnic University) International Workshop on Complex Systems and Networks, Guilin, China, July 2007.
20. “Some Information Technology Applications of Statistical Nonlinear Dynamics,” (invited by Prof. Mustafa Kammash, University of California Santa Barbara, USA), Santa Barbara, November 2006.
21. “An EMI Reduction Methodology Based on Nonlinear Dynamics,” (invited by Prof. Ljiljana Trajkovic, Simon Fraser University, Vancouver, Canada) 3rd International Workshop on Complex Systems and Networks, Vancouver, July 2006.
22. “Some Information Technology Applications of Statistical Nonlinear Dynamics,” (invited by Prof. Ljiljana Trajkovic, Simon Fraser University, Vancouver, Canada), Vancouver, March 2006.
23. “Statistical Approach to Discrete-time Chaotic Systems: Basic Theoretical Tools and Application to EMI Reduction,” Boeing ltd, Seattle, November 2005.
24. “High Throughput True Random Number Generation based on Chaotic Maps," (invited by Prof. M. Tse, Hong Kong Polytechnic University) International Workshop on Complex Systems and Networks, Hong Kong, May 2005.
25. “Chaos-based DS-CDMA: Theoretical Issues and Prototype System Implementation," (invited by Prof. Maciej Ogorzalek, Information Technology Department Chair, Jagellonian University) Jagellonian University, Krakow, Poland, April 2005
26. “A Statistical Approach to Nonlinear Maps with Application to Electrical Engineering” and “An EMI Reduction Methodology Based on Nonlinear Dynamics” (invited by Prof. Malgorzata Chrzanowska-Jeske, EE Department Chair, Portland State University, Portland, OR), Portland State University, Portland March 2005.
27. “Innovative Techniques for EMI Reduction,” (invited by Prof. Alex Stankovic, Northeastern University, Boston, MA), Northeastern University, Boston, USA, August 2004.
28. “A Statistical Approach to Nonlinear Maps with Application to Electrical Engineering,” (invited by Dr. Chai Wah Wu, IBM T. J. Watson Research Laboratories, Yorktown Heights, NY), J. T. Watson Research Laboratories, Yorktown Heights, USA, August 2004.
29. “A Statistical Approach to Nonlinear Maps with Application to Electrical Engineering,” (invited by Dr. G. M. Maggio, STMicroelectronics, San Diego, CA), STMicroelectronics Laboratory, San Diego, USA, August 2004.
30. “Chaos-Based Communication Systems: Introduction, Methodologies and Application to DS-CDMA,” (invited by Dr. Walter Weigel and Dr. Wehrner Mohr, Siemens, Munich, Germany), Siemens, Munich, Germany, January 2004.
31. “Statistical Approach to Discrete-time Chaotic Systems: Theoretical Results and Application to DS-CDMA Communication and EMI Reduction.” (invited by Prof. J. Nossek, Technical University of Munich, Germany and CAS society past-president), Department of EE, Technical University of Munich, Germany, December 2001.
32. “Spread Spectrum Communication Using Chaos,” (invited by Dr. Nikolai Rulkov and Prof. H. Abarbanel, Institute for Nonlinear Science, UCSD, USA), 2000 Winter School in Chaotic Communications, University of California, San Diego, USA, January 2000.
33. “Chaos-Based DS-CDMA,” (invited by Dr. Alban Duverdier, CNES Tolosa, France), during the “Tutorial Day on Signal Processing Using Chaos and its Applications to Telecommunications,” Centre National d'Etudes Spatiales (CNES), Tolosa, France, July 1999.

4.3.3 Tutorials (Invited and Session Organizer)

1. **Tutorial Session Organizer** on “Compressive Sensing: Theory, Applications and Implementation of Secure Nodes for Internet of Things”, *IEEE International Midwest Symposium on Circuits and Systems (MWCAS2019)*, Dallas, USA, August 2019.
2. **Tutorial Session Organizer** on “Compressive Sensing: Theory, Applications and Implementation of Secure Nodes for Internet of Things”, *IEEE International Symposium on Circuits and Systems (ISCAS2017)*, Baltimore, USA, May 2017.
3. **Invited Tutorial** on “Compressive Sensing: Theory, Implementation and Applications”, *IEEE Biomedical Circuits and Systems Conference (BioCAS2016)*, Shanghai, China, October 2016.

4. **Tutorial Organizer** on “Compressive Sensing: From Theory to Circuits and Systems Implementation and Applications,” *IEEE International Symposium on Circuits and Systems (ISCAS2015)*, Lisbon, Portugal, May 2015.
5. **Tutorial Session Organizer** on “Discrete-Time Chaotic Systems: Mathematical Tools and Communication Applications,” *IEEE Global Communications Conference (Globecom2003)*, San Francisco, USA, December 2003.
6. **Invited Tutorial** on “Chaos-Based Code Generation” (invited by Dr. Christopher Patrick Silva, The Aerospace Corporation), *IEEE International Microwave Symposium (IMS2003)*, Philadelphia, USA, June 2003.
7. **Invited Tutorial** on “Tensor Based Analysis of Quantized Chaotic Pseudo-Markov Processes” and “FM-based Generation of high EMC Timing Signals,” *IEEE International Symposium on Circuits and Systems (ISCAS2003)*, Bangkok, Thailand, May 2003.
8. **Invited Tutorial** on “Statistical Modelling of Quantized Discrete Time Chaotic Processes and Application to DS-CDMA Systems Optimization,” *15th European Conference on Circuit Theory and Design (ECCTD01)*, Helsinki, Finland, August 2001.
9. **Tutorial Session Organizer** on “Statistical Approach to Discrete-Time Chaotic Systems: Some Tools for Studying Chaos with Densities and Applications to EMI Reduction,” *IEEE International Symposium on Circuits and Systems (ISCAS2001)*, Sydney, Australia, May 2001.

4.3.4 Special Session Organizer

I have (co)-organized a total of 14 special sessions at a number of different conferences and technical meetings.

1. IEEE Biomedical Circuits and Systems Conference *(BioCAS2011)*, Session on “Compressive Sensing for Biosignals: from Algorithms to Circuits and Systems Design,” San Diego, USA, November 2011.
2. IEEE International Symposium on Circuits and Systems (*ISCAS2010*), Session on “Analysis & Design of Biomolecular Circuits,” Paris, France, May-June 2010.
3. IEEE International Symposium on Circuits and Systems (*ISCAS2009*), Session on “Design of Biological Circuits and Systems,” Taipei, Taiwan, May 2009.
4. International Symposium on Spread Spectrum Techniques and Applications (*ISSSTA2008*), Session on “Statistical Signal Processing,” Bologna, Italy, September 2008.
5. IEEE/IEICE Int. Symposium on Nonlinear Theory and its Applications (*NOLTA2007*), Session on “Complex Systems and Communication Networks,” Vancouver, Canada, September 2007.
6. IEEE European Conference on Circuit Theory and Design (*ECCTD2007*), Session on “Generation and Validation of Random Numbers,” Seville, Spain, August 2007.
7. IEEE/IEICE Int. Symposium on Nonlinear Theory and its Applications (*NOLTA2004*), Session on “Nonlinear and Statistical Signal Processing,” Fukuoka, Japan, November 2004.
8. IEEE International Symposium on Circuits and Systems (*ISCAS2004*), Session on “Nonlinear Dynamics and Complexity in Network Traffic Modelling and Control,” Vancouver, Canada, May 2004.
9. IEEE International Symposium on Circuits and Systems (*ISCAS2003*), Session on “Nonlinear Dynamics for Coding Theory and Network Traffic,” Bangkok, Thailand, May 2003.
10. IEEE International Symposium on Circuits and Systems (*ISCAS2002*), Session on “Statistical Methodologies for Nonlinear Signal Processing,” Phoenix, AZ, USA, May 2002.
11. IEEE/IEICE Int. Symposium on Nonlinear Theory and its Applications (*NOLTA2002*), Session on “Application of Chaos,” Xian, China, October 2002.
12. IEEE/IEICE Int. Symposium on Nonlinear Theory and its Applications (*NOLTA2002*) and Int. Symposium on Information Theory and its Applications (*ISITA2002*), Joint session on “Application of Chaos to Communication and Signal Processing,” Xian, China, October 2002.
13. IEEE/IEICE Int. Symposium on Nonlinear Theory and its Applications (*NOLTA2000*), Session on “Applications of Chaos to Communications and Signal Processing,” Dresden, Germany, September 2000.
14. IEEE/IEICE Int. Symposium on Nonlinear Theory and its Applications (*NOLTA'98*), Session on “Advances in Theory and Implementations of Chaotic Maps,” Crans Montana, Switzerland, September 1998.

5. Honors and Awards

5.1 HONORS

1. **Fellow of the IEEE**, *for contributions to application of nonlinear dynamics to communications, signal processing, and information technology*, 2006. According to what is reported at https://www.ieee.org/membership_services/membership/fellows/index.html, the recognition of IEEE Fellow is a distinction reserved for select IEEE members with extraordinary accomplishments in any of the IEEE fields of interest. It is conferred by the Board of Directors every year to a group of individuals whose total number cannot exceed one-tenth of one percent of the total voting Institute membership.
2. **Distinguished Lecturer,** IEEE Circuits and Systems Society, 2015-2016
3. **Distinguished Lecturer,** IEEE Circuits and Systems Society, 2004-2005.

5.2 PRIZES AND AWARDS

4. **IEEE Transactions on Biomedical Circuits and Systems Best Paper Award**, 2019 (the award recognizes the best paper published in the IEEE Transactions on Biomedical Circuits and Systems which appeared in the years 2016-2018. The award is based on general quality, originality, contributions, subject matter and timeliness). I received this for the paper "Hardware-Algorithms Co-Design and Implementation of an Analog-to-Information Converter for Biosignals Based on Compressed Sensing," *IEEE Transactions on Biomedical Circuits and Systems,* vol. 10, n. 1, pp. 149-162, [J34].
5. **Best Student Paper Award**, 2019 IEEE International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMCCompo2019), Haining, Hangzhou, China. I received this for the paper "Impact of Dead Times on Radiated Emissions of Integrated and Discrete DC-DC Converter," [C26], whose main author was Mr. J. Bačmaga, Ph.D. student of my collaborator Prof. A. Barić (University of Zagreb).
6. **Best Student Paper Award (Gold Leaf)**, 2019 15th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME2019), Lausanne, Switzerland. I received this for the paper "A Practical Architecture for SAR-based ADCs with Embedded Compressed Sensing Capabilities," [C27], whose main author was Mr. Carmine Paolino, current Ph.D. student of mine at Politecnico di Torino.
7. **Best Paper Award Nomination**, 2015 Design Automation & Test in Europe Conference (DATE2015), Grenoble, France. I received this for the paper "An Ultra-Low Power Dual-mode ECG Monitor for Healthcare and Wellness," [C54].
8. **IEEE CAS Society Meritorious Services Award**, 2013, which honors the individual with exceptional long-term service and dedication to the interest of CAS Society, received for *extraordinary leadership in improving timeliness, technical quality, and the reputations of IEEE TCAS-I and IEEE TCAS-II*.
9. **IEEE CAS Society Guillemin-Cauer Award**, 2013 (the award recognizes the best paper published in the IEEE Transactions on Circuits and Systems - Part I or the IEEE Transactions on Circuits and Systems - Part II publications which appeared in the years 2010-2012. The award is based on general quality, originality, contributions, subject matter and timeliness.). I received this for the paper "Rakeness in the design of Analog-to-Information Conversion of Sparse and Localized Signals," *IEEE Transactions on Circuits and Systems – Part I*, vol. 59, n. 5, pp. 1001 – 1014, 2012, [J48].
10. **Best Student Paper Award**, 2011 IEEE International Symposium on Circuits and Systems (ISCAS2011), Rio de Janeiro, Brazil. I receive this for the paper "Analog-to-Information Conversion of Sparse and Non-White Signals: Statistical Design of Sensing Waveforms," [C75], whose main author was Mr. Mauro Mangia, former Ph.D. student of mine at University of Bologna.
11. **Best Paper Award**, 2005 17th European Conference on Circuit Theory and Design (ECCTD2005), Cork, Ireland. I received this for the paper "Chaos-based High-EMC Spread-Spectrum Clock Generator," [C114].
12. **Best Student Paper Award**, 2005 Zurich International Symposium on Electromagnetic Compatibility (EMC Zurich 2005), Zurich, Switzerland. I received this for the paper "A PLL–based Clock Generator with Improved EMC," [C119], whose main authors were Mr. Luca de Michele and Mr. Fabio Pareschi, former Ph.D. students of mine at the University of Bologna.
13. **IEEE CAS Society Darlington Award**, 2004 (award given to the paper published in 2002-2003 in either the IEEE Transactions on Circuits and Systems - Part I or the IEEE Transactions on Circuits and Systems - Part II which better bridges theory and practice). I received this for the paper "Spectral properties of chaos-based FM signals: Theory and simulation results," *IEEE Transactions on Circuits and Systems – Part I,* vol. 50, pp. 3-15, 2003, [J92].
14. **"E. Caianiello" Award,** Best Italian Ph.D. thesis in the field of Neural Networks, 1997.
15. "E. De Castro" Fellowship, Italian Association of Electrical and Electronic Engineers (AEI), 1993.
16. "Gallucci" Award, Best Master Student of the School of Engineering, University of Bologna, 1991.

6. Selected National and International Research Projects

This section reports the research projects, including eventual partners, funded via competitive calls and involving peer review selection, for which I have had or currently have a coordinating role (Principal Investigator (PI), Co-PI, Research Unit Coordinator, …), as well as those stemming from partnership agreements with top-level Electronic and Information Technologies Industries or funded by leading Universities.
Altogether, I have participated in about around 30 projects and have/had a coordinating role in 20 of them. indicated below. Considering only these, the total acquisition was $135M for research, education and facilities funds. It is worth stressing that the most recent projects (since 2010) were either funded by industry, or had a clear focus on applications, which is an indication of my success in the **multidisciplinary approach pairing important theoretical/algorithmic results with** more practical ones focused on **applications and implementation of microelectronic circuits and (embedded) systems**.

6.1 INTERNATIONAL COMPETITIVE RESEARCH PROJECTS

Title: Innovative Signal Processing Exploiting Chaotic Dynamics (Esprit-31103, INSPEC)
Duration: 1998-2001 (36 months)
Role: Co-PI
Funds Institution/Total: €150k/€1M
Funding Institution: European Commission
Partners: University College Dublin (Coordinator) (UCD), Ireland; Swiss Federal Institute of Technology in Lausanne (EPFL), Switzerland; National Microelectronic Center of Seville (CNM), Spain; Helsinki University of Technology (HUT), Finland; Budapest University of Technology and Economics (BME), Hungary; Aristotle University of Thessaloniki (AUT), Greece, as well as Nokia and Analog Devices in the industrial advisory board and University of Ferrara (UNIFE) as subcontractor.

Title: Statistical Aspects of Nonlinear Dynamical Circuits and Systems with Applications to Chaos and Communications Modelling
Duration: 2001-2003 (36months)
Role: Co-PI
Funds Institution/Total: €30k/€60k
Funding Institution: ESPRC (UK)
Partners: University of Birmingham, UK

Title: European Doctorate in Information Technology (MC-EST 504195, EDITH)
Duration: 2004-2008 (48 months)
Role: Co-PI
Funds Institution/Total: €350k/€2M
Funding Institution: European Commission
Partners: DIMES, Delft University of Technology; EPFL-I&C, I & C School, Swiss Federal Institute of Technology, Lausanne; IMEP, Institut National Polytechnique de Grenoble; SCD-K.U.Leuven, EE Dept. (ESAT), Faculty of Engineering (FTW), Katholieke Universiteit Leuven; CEA-LETI, Commissariat à l'Energie Atomique, Laboratoire d'Electronique, de Technologie de l'Information, France; IMEC, Interuniversitair Micro-Elektronica Centrum, Belgium
I entirely wrote the proposal which was granted an overall fund of over 2M€ after a particularly selective process in which only 7% of 750 submitted proposals were funded.

Title: Wireless Sensor Networks: From Theory To Practical Applications (Exploratory Phase)
Duration: 2004 (6 months)
Role: PI
Funds Institution/Total: €7k/€30k
Funding Institution: NATO
Partners: University "Cyril & Methodius," Skopje, Macedonia; University of California San Diego, USA

Title: Application of Nonlinear Dynamics to Information Technology (Interlink II04C050E9, ACASTI)
Duration: 2004-2010 (78 months)
Role: PI
Funds Institution/Total: €90k/€200k
Funding Institution: MIUR
Partners: Queen Mary University of London, UK; Swiss Federal Institute of Technology in Lausanne (EPFL), Switzerland; IBM, T. J. Watson Research Laboratories, USA; University of California San Diego

(UCSD), USA; Northeastern University, Boston, USA; STMicroelectronics, Wireless Research Center, Geneva, Switzerland; University of Washington, Seattle, USA; Katholieke Universiteit Leuven, Belgium

Title: Modelling, Control and Management of Thermal Effects in Electronic Circuits of the Future (THERMINATOR)
Duration: 2010-2013 (48 months)
Role: Co-PI
Funds Institution/Total: €80k/€5M
Funding Institution: European Commission
Partners: STMicroelectronics, Infineon Technologies, NXP Semiconductors, ChipVision Design System, Gradient Design Automation, MunEDA, Synopsys, Budapest University of Technology and Economics, Centre Suisse d'Electronique et de Microtechnique, Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung, Interuniversitair Micro-Electronica Centrum Belgium, Commisariat a l'Energy Atomique, OFFIS Germany, Politecnico di Torino Italy, Alma Mater Studiorum - Università di Bologna Italy

Title: Energy to Smart Grids (ENIAC-ED-52 v161210, E2SG)
Duration: 2012-2015 (36 months)
Role: Co-PI
Funds Institution/Total: €252k/€33.5M
Funding Institution: ENIAC JU
Partners: Austriamicrosystems; Centre Tecnològic de Telecomunicacions de Catalunya; Centro Ricerche FIAT; Fraunhofer IISB; HELIOX; HERA; Infineon Technologies; IQE Silicon, Spain; IQUADRAT; Italian Universities NanoElectronics Team (IUNET – Unife is part of it); LEITAT; METATRON; NXP Germany; NXP Semiconductors; On Semiconductor; POLIMODEL; Politecnico di Torino; R-DAS; RWTH Aachen University; Silvaco; Slovak University of Technology; STMicroelectronics Italy; Telefunken Semiconductors; TP Vision Netherlands; University of Bologna; University of Calabria; University of Catania; University of Sheffield

Title: Innovative smart components, modules and appliances for a truly connected, efficient and secure smart grid (H2020-ECSEL-737434-2, CONNECT)
Duration: 2017-2020 (36 months)
Role: Co-PI
Funds Institution/Total: €82k/45M
Funding Institution: EC-ECSEL JU
Partners: Infineon Technologies AG, NXP SEMICONDUCTORS Germany GMBH, Friedrich Alexander Universität Erlangen, Rheinisch-Westfaelische Technische Hochschule Aachen, Devolo AG, Mixed Mode GmbH, Slovenska Technicka Univerzita v Bratislave, R-DAS SRO, Enexis BV, Philips Electronics Nederland B.V., Technische Universiteit Eindhoven, Heliox BV, GreenFlux, Abengoa Research, Acondicionamiento Tarrasense Associacion, Centre Tecnologic De Telecomunicacions De Catalunya, Iquadrat Informatica SL, STMICROELECTRONICS SRL, ENEL Distribuzione S.P.A., Consorzio Nazionale Interuniversitario Per La Nanoelettronica (IUNET – Unife is part of it), Politecnico di Bari

Title: Frictionless Energy Efficient Convergent Wearables for Healthcare and Lifestyle Applications (FLAG–ERA JTC, CONVERGENCE)
Duration: 2017-2020 (36 months)
Role: Co-PI
Funds Institution/Total: €45k/€15.5M
Funding Institution: ENIAC JU
Partners: Ecole Polytechnique Fédérale Lausanne, Eidgenössische Technische Hochschule Zürich, Consorzio Nazionale Interuniversitario Per La Nanoelettronica (IUNET – Unife is part of it), Italian National Agency for New Technologies, Energy and Sustainable Economic Development, Università Campus Bio-Medico di Roma, Università degli Studi di Cagliari, TAgliaferri SrL, Institut Polytechnique de Grenoble, Commissariat à l'Energie Atomique, STMicroelectronics, Université catholique de Louvain, Elektronikas un datorzinatnu instituts, National Institute for R&D Microtechnologies, Universitatea Transilvania din Braşov, Hirslanden Clinic Cecil, Tallinn University of Technology, Middle East Technical University, Turkey

Title: Highly efficient and trustworthy electronics, components and systems for the next generation energy supply infrastructure (PROGRESSUS)
Duration: 2020-2022 (36 months)
Role: Co-PI
Funds Institution/Total: €75k/€20M
Funding Institution: EC-ECSEL JU

Partners: Infineon Technologies AG, Devolo AG, Mixed Mode GMBH, Ceus UG, Friedrich-Alexander-Universitaet Erlangen-Nuernmebrg, Fachhochschule Köln, Enexis Personeel BV, Stichying Elaadnl, Heliox BV, Greenflux Assets B.V., Technische Universiteit Eindhoven, Technische Universiteit Delft, Iquadrat Informatica SL, Hybrid Energy Storage Solutions, CTC, Acondicionamiento Tarrasense Associacion, STMICROELECTRONICS SRL, ENEL X Srl., Consorzio Nazionale Interuniversitario Per La Nanoelettronica (IUNET – Polito is part of it), Politecnico di Bari, Slovenska Technicka Uverzita Bratislave, R-DAS, s.r.o.

Title: Embedded storage elements on next MCU generation ready for AI on the edge (STORAIGE)
Duration: 2021-2024 (36 months)
Role: Co-PI
Funds Institution/Total: €550k/€10M
Funding Institution: EC-ECSEL JU
Partners: STMicroelectronics, Commissariat à l'Energie Atomique et aux à Energies Alternatives, Interuniversitair Micro- Electronica Centrum, CSEM Centre Suisse D'electronique Et De Microtechnique Sa - Recherche Et Developpement, Cybertron Tech Gmbh, Institut Mikroelektronickych Aplikaci, Ustav Teorie Informace A Automatizace, Fraunhofer, X-FAB, Technische Universitat Darmstadt, IMMS Institut Fuer Mikroelektronik- Und Mechatronik-Systeme, EDC Electronic Design Chemnitz, Micro-Sensys, Knowtion, Endiio Engineering, Emmtrix Technologies, Universite Grenoble Alpes, Soitec, Thales, Universite D'aix Marseille, Pfeiffer Vacuum, Politecnico di Torino, Consorzio Nazionale Interuniversitario Per La Nanoelettronica (IUNET) , Strikersoft, Kungliga Tekniska Hoegskolanuppsala Universitet, Atlas Copco Industrial Technique, Turkiye Bilimsel Ve Teknolojik Arastirma Kurumu, Tubitak, Ford Otomotiv Sanayi, Turkcell Teknoloji Arastirma Ve Gelistirme, Buyutech Teknoloji Sanayi Ve Ticaret, Arcelik, Istanbul Medipol Universitesi Vafki, Zf Friedrichshafen, Melexis

Title: Failure identification with on-board prediction by artificial intelligence (FIORIRE)
Duration: 2022-2023 (18 months)
Role: Co-PI
Funds Institution/Total: €120k/€800k
Funding Institution: European Space Agency (ESA)
Partners: University of Bologna, Thales Alenia Space, Leonardo, ALTEC

6.2 National Competitive Research Projects

Title: Methods for the Statistical Characterization of Nonlinear Dynamical Systems with application to Information and Electrical Engineering
Duration: 2003-2006 (45 months)
Role: Co-PI
Funds Institution/Total: €175k/€300k
Funding Institution: MIUR
Partners: University of Bologna

Title: Theoretical performance limits of chaotic spreading sequences in DS-CDMA systems
Duration: 2003-2005 (36 months)
Role: Co-PI
Funds Institution/Total: €70k/€70k
Funding Institution: MIUR
Partners: N/A

Title: Innovative Methodologies for Analysis and Design of Chaotic Circuits
Duration: 2002-2006 (48 months)
Role: PI
Funds Institution/Total: €150k/€620k
Funding Institution: MIUR
Partners: University of Genoa, Polytechnic of Milan, Politecnico di Torino

6.3 Industry-Funded Research Projects

Title: Chaos-based spread-spectrum timing signal generation for EMI reduction in switching power converters (REDEMI)
Duration: 2010-2011 (18 months)
Role: PI

Funds Institution/Total: €48k/€48k
Funding Institution: National Semiconductor
Partners: National Semiconductor

Title: Innovative Circuits Solutions for Biological Signal Processing Exploiting Compressive Sensing (BIOCOMP)
Duration: 2011-2012 (24 months)
Role: PI
Funds Institution/Total: €64k/€64k
Funding Institution: Texas Instruments
Partners: Texas Instruments

Title: Innovative Design Methodologies for Bi-directional Power-line Communication in Isolated Resonant Switching Converters (IDeM2CIRC)
Duration: 2015-2017 (24 months)
Role: PI
Funds Institution/Total: €100k/€100k
Funding Institution: Texas Instruments
Partners: Texas Instruments

Title: Design Methodologies for Low-EMI Switching Power Converters for Automotive (LESCA)
Duration: 2022-2023 (18 months)
Role: PI
Funds Institution/Total: €100k/€100k
Funding Institution: STMicroelectronics
Partners: STMicroelectronics

6.4 RESEARCH PROJECTS FOUNDED BY LEADING UNIVERSITIES

Title: Design and Implementation of Ultra-low-power IoT Nodes (ULIoT)
Duration: 2017-2021 (48 months)
Role: PI
Funds Institution/Total: €250k/€250k
Funding Institution: Politecnico di Torino
Partners: N/A

7. Publications

In summary, I am (co)-author of over 340 scientific publications summarized in the table below

Type of Publication	Total
Patents (Italian)	2
Books (Edited or Authored)	5
International Journals with Peer Review (**of which IEEE Journals**)	101 (**74**)
International Conferences with Peer Review (**of which invited contributions**)	220 (**26**)
Book Chapters	12
Special Issues/Sections of Journals (Guest Editor)	9

My research activity is highly multidisciplinary and has been published in 19 different IEEE journals sponsored by nine (9) different IEEE Societies/Councils (Circuits and Systems; Communication; Computer; Electron Devices; Engineering in Medicine and Biology; Power Electronics, Sensors; Signal Processing; System Man and Cybernetics). My contributions have received **best paper awards from three journals** — the IEEE Transactions on Circuits and Systems – Part I, the IEEE Transactions on Circuits and Systems – Part II, and the IEEE Transactions on Biomedical Circuits and Systems in 2004 (IEEE CAS Society Darlington award), in 2013 (IEEE CAS Society Guillemin-Cauer award) and 2019 (IEEE Transactions on Biomedical Circuits and Systems Best Paper Award), as well as the **best paper award** at ECCTD2005 and the **best paper award nomination** at DATE2015. I was also the co-recipient of **four best student paper awards** at EMCZurich2005, IEEE ISCAS2011, IEEE PRIME2019 and EMCCompo2019.
Furthermore, Journal articles [J76] and [J81] have been evaluated as **class A/"excellent"** in the Italian CIVR2001-2003 research evaluation exercise, while [J58], [J60], [J61], [J67] and [J70] have been evaluated as **class A/"excellent"** in the VQR2004-2010 research evaluation exercise, and [J43], [J48] and [J49] have been evaluated as **class A/"excellent"** in the VQR2011-2014, as well as [J21], [J23], [J26], [J29], [J34], [J36], [J41] have been evaluated as **class A/"excellent and extremely relevant"** in the VQR2015-2019.[4]
In terms of impact of the results of the research activity, according to Scopus as of December 8, 2023, I received 4477 citations, with an Hirsch index of 34. If one includes also the book [B4] which is not indexed by Scopus, adding the number of citations for it reported by Google Scholar, the citation count would increase to 4935 with $h = 35$.

The complete list of publications is reported blow in the following order

- Books
- Chapters in collected Books with Peer Review
- Contributions in Peer Reviewed Journals
- Contributions in Proceedings of International Conferences with Peer Review
- Edited Special Issues
- Patents

7.1 BOOKS

B1 M. Mangia, F. Pareschi, V. Cambareri, R. Rovatti, G. Setti, "Adapted Compressed Sensing for Effective Hardware Implementations", *Springer*, 2017 (ISBN 978-3-319-61372-7, DOI: 10.1007/978-3-319-61373-4)

B2 H. Koeppl, D. Densmore, G. Setti, M. Di Bernardo (Eds), "Design and Analysis of Biomolecular Circuits," *Springer*, 2011 (ISBN 978-1-4419-6765-7)

B3 A. Tasic, W. Serdijn, L. Larson, G Setti (Eds.), "Circuits and Systems for Future Generations of Wireless Communications," *Springer*, 2009 (ISBN: 978-1-4020-9918-2)

B4 M. P. Kennedy, R. Rovatti, G. Setti, (Eds.) "Chaotic Electronics in Telecommunications," *CRC Press*, Boca Raton, USA, 2000 (ISBN 0-8493-2348-7)

B5 G. Setti, R. Rovatti, G. Mazzini (Eds.), "Proceedings of the 8th IEEE International Specialist Workshop on Nonlinear Dynamics of Electronic Systems" (NDES2000), *World Scientific*, Singapore, 2000 (ISBN 981-02-4341-3)

[4] Class A correspond to the highest possible score in the research evaluation exsercise.

7.2 BOOK CHAPTERS

BC1 F. Pareschi, G. Setti, S. Callegari, R. Rovatti, “Implementation of low EMI Spread Spectrum Clock Generators Exploiting a Chaos-based Jitter,” in Intelligent Computing Based on Chaos, L. Kocarev, Z. Galias, S. Lian (Eds.), pp. 145-172,Springer-Verlag, 2009.

BC2 F. Pareschi, S. Callegari, G. Setti, , R. Rovatti, “Circuits and systems for the synthesis of chaotic signals in engineering applications,” in Intelligent Computing Based on Chaos, L. Kocarev, Z. Galias, S. Lian (Eds.), pp. 173-196, Springer-Verlag, 2009.

BC3 S. Callegari, R. Rovatti, G. Mazzini, G. Setti, “A Chaos Approach to Asynchronous DS-CDMA Systems,” in Chaos Applications in Telecommunications, Peter Stavroulakis (Ed), CRC Taylor an Francis, pp. 173-206, 2006.

BC4 G. Setti, R. Rovatti, G. Mazzini, “Chaos-Based Generation of Artificial Self-Similar Traffic,” in Complex Dynamics in Communication Networks, L. Kocarev, G. Vattay (Eds), pp. 159-190, Springer-Verlag, 2005.

BC5 G. Setti, R. Rovatti, G. Mazzini, “Control of Chaos Statistics for Optimization of DS-CDMA Systems,” in Chaos and Bifurcation Control: Theory and Applications, G. Chen, D. J. Hill, X. Yu (Eds), pp. 295-319, Springer-Verlag, Berlin, 2003.

BC6 G. Setti, R. Rovatti, S. Callegari, M. Balestra, “Control of Chaos Statistics for the Generation of Timing Signals with Improved EMC,” in Chaos and Bifurcation Control: Theory and Applications, G. Chen, D. J. Hill, X. Yu (Eds), pp. 341-369, Springer-Verlag, Berlin, 2003.

BC7 G. Mazzini, R. Rovatti, G. Setti, “Chaos-Based Asynchronous DS-CDMA Systems,” in Chaotic Electronics in Telecommunications, M. P. Kennedy, R. Rovatti, G. Setti (Eds.), pp. 33-79, CRC Press, Boca Raton, Florida, 2000.

BC8 S. Callegari, R. Rovatti, G. Setti, “Robustness of Chaos in Analog Implementations,” in Chaotic Electronics in Telecommunications, M. P. Kennedy, R. Rovatti, G. Setti (Eds.), pp. 397-442, *CRC Press*, Boca Raton, Florida, 2000.

BC9 S. Graffi, G. Setti, “Network Analysis Using Linearization,” Wiley Encyclopedia of Electrical and Electronics Engineering (J. Webster Ed.), *John Wiley & Sons*, New York, USA, vol. 14, pp. 107-114, 1999.

BC10 G. Setti, P. Thiran, C. Serpico, “An Approach to Cellular Neural Networks for Signal Processing: Information Propagation and Circuit Design,” in Neural Nets, M. Marinaro and R. Tagliaferri (Eds.), Perspective in Neural Computing Series, *Springer-Verlag*, London, U.K., pp. 83-99, 1999.

BC11 R. Rovatti, A. Bellini, G. Setti, E. Franchi and N. Manaresi, “Automatic Implementation of Analog Chaotic Generators as Fuzzy Systems,” New Trends in Fuzzy Logic II, P. Blonda, et al. (Eds.), pp. 203-210, World Scientific, Singapore, 1998.

BC12 C. Serpico, G. Setti, P. Thiran, “Analogies Between Cellular Neural Networks and Partial Differential Equations,” Advances in Intelligent Systems - Frontiers in Artificial Intelligence and Applications, IOS Press, pp.157-162, 1997.

7.3 ARTICLES IN PEER REVIEWED JOURNALS

J1 A. Celentano, C. Paolino, F. Pareschi, L. Callegaro, R. Rovatti and G. Setti, “Mutual Inductance Measurement in Wireless Power Transfer Systems Operating in the MHz Range,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2024, DOI: 10.1109/TCSII.2023.3334432.

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7.5 SPECIAL ISSUES/SECTIONS

S1 J. M. De La Rosa, G. Setti, (Guest Eds.) Special Issue on “ISCAS 2018”, *IEEE Transactions on Circuits and Systems – Part II,* May 2018

S2 M. di Bernardo, E. da Silva, P. Häfliger, Gianluca Setti, (Guest Eds.) Special Issue on “ISCAS 2015”, *IEEE Transactions on Circuits and Systems – Part I,* May 2016.

S3 M. di Bernardo, Y. Lian, W. Serdijn, G. Setti, (Guest Eds.) Special Issue on “ISCAS 2014,” *IEEE Transactions on Circuits and Systems – Part I,* May 2015.

S4 S. Renaud, G. Setti, R. F. Yazicioglu, (Guest Eds.) Special Issue on “Selected Papers from IEEE BioCAS 2013,” *IEEE Transactions on Biomedical Circuits and Systems*, October 2013.

S5 D. Allstot, R. Rovatti, G. Setti, (Guest Eds.) Special Issue on “Circuits, Systems and Algorithms for Compressive Sensing,” *IEEE Journal on Selected and Emerging Topics in Circuits and Systems*, September 2012.

S6 A. C. Carusone, Y. Ismail, U. Moon, H. Schmid, W. Serdijn, G. Setti, (Guest Eds.) Special Issue on “ISCAS 2008,” *IEEE Transactions on Circuits and Systems – Part I,* May 2009.

S7 G. Setti, T. Ushio (Guest Eds.), Special Section on “Nonlinear Theory and its Applications,” *IEICE Transactions on Fundamentals*, October 2007.

S8 K. Nakano, G. Setti (Guest Eds.), Special Section on “Multi-dimensional Mobile Information Networks,” *IEICE Transactions on Fundamentals*, July 2006.

S9 M. Hasler, G. Mazzini, M. Ogorzalek, R. Rovatti, G. Setti, (Guest Eds.), Special Issue on “Applications of Nonlinear Dynamics to Electronic and Information Engineering,” *Proceedings of the IEEE*, May 2002.

7.6 PATENTS

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8. Detailed Description of Main Research Interests

My research activity is **multidisciplinary in nature**, which is also demonstrated by the facts that:

- I have received the scientific habilitation (which is a necessary condition for promotion from Assistant to Associate and to Full Professor in Italy) **in three different scientific areas** ("SSD"): Electrotechnology (ING-IND/31, Elettrotecnica), Electronic Engineering (ING-INF/01, Elettronica), Computer Engineering (ING-INF/05 Sistemi di Elaborazione delle Informazioni);
- I have publishedarticles in **19 different** IEEE Transactions/Journals sponsored by **9 different IEEE societies/councils** (Circuits and Systems; Communication; Computer; Electron Devices; Signal Processing; System Man and Cybernetics; Engineering in Medicine and Biology; Sensors; Power Electronics).

More specifically my scientific efforts range from the areas of neural networks and nonlinear (statistical-)dynamical systems theory, statistical signal processing (particularly compressed sensing algorithms for IoT nodes), (statistical)algorithms-hardware co-design of integrated systems, and (embedded) systems for biomedical signal (EEG, ECG, EMG, …) processing and wellness, to switching power converters (mainly design of IC-friendly class-E power converters and defining system level methodologies to reduce their EMI signature), and embedded systems security (random number generators of cryptography, analysis and design of low-complexity information security schemes based on compressed sensing). Most recently I also moved to Tiny Machine Learning applied to the use of low-cost/low-energy embedded systems for anomaly detection

The five areas in which my research activity has had the most significant impact so far include:

- Nonlinear Signal Processing and Statistical Algorithms for (Integrated) Circuits/Systems Optimization
- Compressed Sensing for Biomedical Signal and Processing and IoT nodes: Algorithms, Architectures and Implementation
- Switching power converters
- Embedded Systems Security
- Information Processing in Artificial Neural Networks

For each of the five areas I describe the corresponding timeframe, the main collaborators (highlighting those who are in my research group), and a detailed description of the rationale and main contribution of my research activity in the context of the results available in the scientific community. When doing so, I have also highlighted and commented on the most significant papers in each area.

8.1 NONLINEAR SIGNAL PROCESSING AND STATISTICAL ALGORITHMS FOR (INTEGRATED) CIRCUITS/SYSTEMS OPTIMIZATION

Timeframe: This research activity originated during my stay at EPFL and was carried out mainly after my Ph.D. (from late 1996).

The main collaborators, belonging to my research group, are/have been Prof. Riccardo Rovatti (Professor of Electronics since 2013 at the University of Bologna, Italy) Prof. Gianluca Mazzini (Associate Professor of Telecommunications since 2002 at the University of Ferrara, Italy), and Prof. Sergio Callegari (Former Student and now Associate Professor of Electronics since 2017 at the University of Bologna, Italy).

I also have/had collaborations with Dr. Gian Mario Maggio (when he was working for STMicroelectronics, San Diego), Prof. Ljupco Kocarev (UCSD), Prof. Tohru Kohda (when he was at Kyushu University, Japan), Prof. Antony Lawrance (when he was at Warwick University, UK), Prof. David Arrowsmith (when he was at Queen Mary University of London, UK), Prof. Michael Peter Kennedy (University College Dublin, Ireland).

Rationale and contribution: Many problems in modern Information and Communication Technology (ICT) can be modelled by the interaction of a (often very complex) stochastic process (e.g. noise, interference, traffic, computation requests, etc.) with one or more artificial devices. In such a general framework, the performance of the resulting system can be expressed as a function of the parameters characterizing the artificial devices as well as of the features of the stochastic process. Hence, any truly optimal design procedure must entail a deep understanding of how these "stochastic algorithms" influence the system performances, as well as the possibility of synthesizing stochastic processes with pre-determined features.

One of my most impactful papers [J81] presents a tutorial overview of the methods of Statistical Dynamical System Theory (SDST) which have expanded the role of stochastic methods in engineering design as well as hardware-algorithm co-design. In fact, it shows how, under suitable assumptions, some physical and

possibly artificial systems exhibit an evolution that may be effectively predicted and thus designed by means of stochastic methods. In Paper [J81] (as well as in [J82], [J88] and [J89]) I and my research group **proposed a general formal theory** that, by exploiting the chaotic dynamics of simple nonlinear 1-D maps, allows the analysis and the synthesis of finite-valued stochastic processes with exponential memory (such as, but not limited to, those produced by Markov chains). More specifically, the papers introduced a systematic tensor-based computation which provides a complete characterization of the process generated by 1-D chaotic maps in terms of moments of any order. In [J81] and [J82], I also showed the very important result that the above analysis procedure can reversed into a synthesis mechanism which can be considered a true **methodology of (stochastic-)algorithm-hardware co-design**: one can design 1-D maps to be used *as process generators with tunable statistics*, which can be exploited in the general procedure for the design/optimization of any ICT system/application which has been described in my research statement which is the key in the practical application of SDST.

It is also notable that [J81] was evaluated as **excellent** in the Italian research evaluation exercise CIVR2001-2003.

The general procedure mentioned above and based on the results of paper [J81] was applied also in two of my other key contributions, i.e. [J67] and (in a more rudimentary form) [J99], to obtain the results highlighted below, which had a very significant impact in the scientific community. It is worth stressing that, while not related to the use of chaotic maps, the same approach of stochastic-algorithm-hardware co-design is the basis for the results reported in two more recent key papers of mine, i.e. (see section 2 below) [J48] (recipient of **the 2013 IEEE CAS Society Guellemin-Cauer Award** and evaluated as **excellent** in the Italian research evaluation exercise VQR2011-2014) and [J34] (recipient of **the 2019 IEEE Transactions on Biomedical Circuits and Systems Best Paper Award**).

Paper [J99] is my first paper dealing with the use of chaotic dynamics to optimize spread spectrum communications based on Direct Sequences Code Division Multiple Access (DS-CDMA) techniques in an asynchronous environment. In [J99], I introduced for the first time the idea of using quantized chaotic sequences to replace classical pseudo-random (i.e. m-, Gold, Kasami…) sequences for spectrum spreading. Furthermore, I was able to show that practical performance improvements were achievable, while in a companion paper (see [J98]) I was able to prove theoretically that the use of chaos-based spreading sequences cannot lead to worse performance that classical pseudo-random ones. These results were very important since they **introduced the only case in which the application of chaos to communication resulted in improved performance with respect to classical solutions.** This contribution was particularly appreciated by the scientific community as proven by the **457 citations** which papers [J99] and [J98] have cumulatively received according to Scopus. It is also worth stressing that, despite having been obtained several years ago, these results remain relevant, since they **can be applied in the design of ultra-low-power sensing nodes for IoT**. In fact, the (stochastic-)algorithm-hardware co-design methodology can be applied, when the number of nodes is fixed, to achieve a desired communication quality **while reducing**, with respect to a classical solution, the length of the necessary spreading sequences and therefore **the energy necessary for information transmission**.

The main additional results obtained in this area are described below.

- Paper [J92]: I was able to show that when spreading sequences are generated by a suitable chaotic map, one is able to achieve the ***absolute minimum*** multiple-access interference. Hence, when multiple-access interference is the main cause of errors in the communication, chaos-based spreading allows one to obtain the optimum system performance, which can be computed to have ***an average 15.47% (and optimized 60% peak value) increase*** in "user capacity" (i.e., the number of users that can access the system with the same communication quality) with respect to systems adopting random or pseudo-random spreading. This is an optimum result, in the sense that no other choice of sequence generation policy can result in a lower interference.
- Paper [J84]**:** Here theoretical predictions have been confirmed by a prototype system comprising of 8 transmitters and a receiver matched with one of the transmitters. This was an important achievement since it was the ***first implementation*** of a chaos-based communication system prototype that outperforms the equivalent one employing standard methodology.
- Paper [J91]**:** Chaos-based spreading has here been proven to **enhance by at least 10%** the system performance in terms of lost bits in the sequence acquisition phase at link startup and also in terms of corresponding delay to service.
- Paper [J70]**:** With the aim of moving investigations toward practical implementation of chaos-based DS-CDMA systems, I studied here the effects of using spreading sequence pulses which are not rectangular as assumed in theory. I was able to show for the first time that a joint optimization of

spreading sequence statistical features and shape of the chip pulses allows ***an improvement of up to 16% in user capacity*** over traditional systems.

This paper was evaluated as **excellent** in the Italian research evaluation exercise VQR2004-2010.

- Paper [J61]**:** This reports a chaos-based sequence generation method for reducing multiple access interference in DS ultra-wide-band wireless-sensor networks (WSNs). The contribution is important since it shows that it is possible to increase the expected bit rate (BR) at which each user may transmit given a certain link quality, measured as the signal-to-interference ratio. When compared with traditional random sequences, chaos-based spreading results **in a BR increase of up to 20%.** This papers can also be considered the key for the application of this method in the **design of ultra-low-power IoT nodes**.

  This paper was also evaluated as **excellent** in the Italian research evaluation exercise VQR2004-2010.
- Book [B4]: The book is very important since it represent the first comprehensive and systematic collection of all techniques dealing with chaos-based communication systems, both at code- signal-, and circuit-level. Despite having been published in 2000, it truly still represents an important reference in its field, as shown by the fact that it is still sold and well cited today and has received overall **428 citations** according to Google Scholar.

8.2 COMPRESSED SENSING FOR BIOMEDICAL SIGNAL PROCESSING AND IOT NODES: ALGORITHMS, ARCHITECTURES AND IMPLEMENTATION

Timeframe: This research was initiated during my visit at EPFL in 2005 for the Summer Research Institute, where I was exposed to Compressed Sensing by following a seminar held by Vivek Goyal.
The activity is still ongoing and where I am focusing a significant part of my current activity. The main collaborators belonging to my research group are Prof. Riccardo Rovatti (Professor of Electronics since 2013 at the University of Bologna, Italy), Prof. Mauro Mangia (former PhD students and now Assistant Professor at the University of Bologna, Italy) and Prof. Fabio Pareschi (former PhD students and now Associate Professor at the Politecnico di Torino, Italy). It is also worth mentioning the industrial interest by TI on this topic (group led by Dr. Giovanni Frattini, now with Analog Devices), for which I have received funds to develop a prototype of **Analog-to-Information Converters based on CS for biomedical signal acquisition and IoT applications**. I also had a collaboration with Prof. Pamela Abshire and Prof. Jonathan Simon, University of Maryland, USA, in the area of **CS applications for Wellness** and, in particular, to develop a CS-based, low-cost, low-power EEG acquisition and recording system for schizophrenic patients. In the same timeframe, I have also collaborated with the research group of Prof. Luca Benini (University of Bologna, Italy and ETHZ, CH) in the area of **CS applications in embedded systems.** Most recently I have started a collaboration with Prof. Wouter Serdijn (Technical University of Delft, The Netherlands), again in the area of **biomedical systems**, for exploiting CS in the design of a new generation of systems for acquisition of Atrial ECG during open-heart surgery.

Rationale and contribution: Conventional approaches to sample and capture signals or images are based on the celebrated Shannon theorem stating that the sampling rate must be at least twice the highest frequency in the band of the signal (the Nyquist frequency). This principle is the basis of almost all methods of acquisition used in audio and video consumer devices, in the processing of medical images, operation of radio receivers, etc.; indeed, classical analog-to-digital conversion is based on this approach and signals are sampled at the Nyquist frequency or higher. Compressed sensing (CS) is a new paradigm for the acquisition/sampling of signals that violates the intuition behind the theorem of Shannon. In fact, CS theory states that, under surprisingly broad conditions, it is possible to reconstruct certain signals or images using far fewer samples or measurements than with traditional methods. To enable this, CS is based on two concepts/principles: *sparsity*, which is related to the signals of interest, and *incoherence*, which is linked to the methods of measurement/acquisition/sampling. Sparsity expresses the idea that the information rate of a signal can be much less than what is suggested by its band, or, for a discrete-time signal, that the number of its degrees of freedom may be much smaller than its time-length. More specifically, CS uses the fact that many natural signals have a very small representation when expressed in an appropriate basis, i.e. that if one indicates with B a matrix collecting appropriate basis vectors, every possible realization of the signal is obtained as a product $B\alpha$ where α is a vector with a (very) small number of non-zero entries. Incoherence expresses the idea that the linear operator processing the signals of interest to extract the samples, does not favor any of the vectors in the sparsity basis thus making all samples fully representative of any possible sparse vector. Practically speaking, incoherence can be assured by projecting the signal to be acquired on a random Pulse Amplitude Modulation (PAM) signal with i.i.d. symbols. Based on these concepts, it is possible to devise protocols for sampling/measurement which capture the information content, but **require a number of measurements comparable to the number of non-zero coefficients in the expression of the signal**

of interest with respect to its sparsity basis. In fact, it can be proved that, under very general conditions, a sufficiently sparse linear representation can be correctly and efficiently retrieved by convex optimization. These results have already caused a small revolution in the signal processing community, since they have offered a completely new perspective in fundamental assumptions such as the sampling bound and the choice of the basis for the signal representation.

A first important contribution to this area is the one that I consider **one of my key contributions to this topic** [J48], where I introduced the concept of *rakeness,* as additional design criteria for the acquisition sequences. This can be applied when the signals, in addition to being sparse, are also *localized*, i.e. when their energy preferentially occupies a given subspace (for instance they are all low-pass in the frequency domain). Maximizing rakeness will help to increase the energy of the samples collected during the acquisition phase and thus the average SNR used in signal reconstruction. Yet, such a maximization cannot be unconstrained, since the property of incoherence needs to be satisfied too. The methodology proposed in Paper [J48], which can also be considered as an instance of **(stochastic-)algorithm-system co-design** (see section 1), resolves this conflict and achieves an improvement in the average SNR of the reconstructed signals of at least 4dB with respect to the classical CS, which correspond to the need for 50% less samples for the same quality of the reconstructed signal. It is worth stressing that this concept has been recognized by the community by awards and citations: [J48] is the follow up of [C75] and [C80] which have received 16 and 14 citations respectively, resulting in a total of **106 citations**, according to Scopus; furthermore, Paper [J48] has also received the **IEEE CAS Society Guillemin-Cauer award** in 2013 and was also evaluated as **excellent** in the VQR2011-2014 Italian research evaluation exercise.

Furthermore, I and my research group also studied the possibility of implementing a prototype of a (biomedical) signal acquisition system based on CS (called Analog-to-Information or A2I converter). Paper [J47] represents the **first detailed comparison** between different A2I architectures to highlight their pros and cons and to present suitable design strategies for all of them. This comparison was also the basis for the design and implementation of our first A2I prototype in collaboration with TI which is reported in [J34]. In this work, I contributed to the chip design and was also responsible for devising a test procedure, which is one of the most important parts of the paper, since it is completely innovative (A2I converters cannot, in fact, be tested as normal signal acquisition systems based on A/D converters). This paper is also very important since it clearly shows the advantages of using the theoretical results in paper [J48] to minimize the complexity of the necessary hardware, that is, **it clearly highlights the necessity of performing algorithm-hardware co-design to maximize the impact of A2I converters**. Also this activity was very well received by the scientific community as shown by the fact that it has received the **2019 IEEE Transactions on Biomedical Circuits and Systems Best Paper Award** in addition to 74 citations according to Scopus.

Additional important results have been recently obtained in the use of CS as a (statistically tunable) compression algorithm to be **employed in embedded systems to reduce either the impact of data storage in memories or the energy used for signal transmission, or both**.

In paper [J39] I have proposed the use of an embodiment of CS as a lossy digital signal compression, whose encoding stage only requires a number of fixed-point accumulations that is linear in the dimension of the encoded signal. More specifically [J30] shows that when (i) a scalar quantiser is used to reduce the measurements' bit-rate, (ii) Huffman Coding (HC) is applied on the encoded bitstream, (iii) rakeness as proposed in [J48] is used to statistically tune acquisition to the family of signals, the attained code rates and recovery Signal-to-Noise Ratio (SNR) performances of a CS-based Digital Signal Compressor are optimized and perform better than standard compression schemes.

In paper [J40], I and my research group demonstrated the advantages of *punctured* CS, i.e. CS acquisition where randomly chosen samples are simply not acquired by switching off both the analog front-end and the analog-to-digital converter. We showed that reconstruction of acquired bio-signals is possible at a level conventionally defined by medical Doctors as "very good" if puncturing is applied to as many as 40% of the samples; this very much reduces the energy footprint of the corresponding acquisition node and make CS **truly well suitable for IoT applications.**

Paper [J15] studied the problem of reconstruction of signals acquired using CS in the case of wellness applications, i.e. when the embedded systems implementing the signal gateway (in which the reconstruction algorithm is running) is battery powered and needs therefore to satisfy tight energy constraints. We have studied the **energy cost and real-time reconstruction feasibility on the gateway**, considering different signal reconstruction algorithms running on a heterogeneous mobile SoC based on the ARM big.LITTLE™ architecture. The important result is that, while standard CS acquisition cannot satisfy real-time constraints, rakeness-based CS prosed in [J40] enables different QoS-energy trade-offs and makes the CS decoding task suitable for wearable devices oriented to long-term ECG monitoring.

What is reported in paper [J16] is important since it shows that **rakeness-based CS can be applied to optimize the overall design of a communication network involving a large number of IoT nodes**. In particular, [J23] considers a distributed IoT data acquisition scenario, where a large number of nodes must send their information to a central collector which may be far from the data acquisition point. Hence, readings from individual nodes may reach their destination by exploiting both local and long-range

transmission capabilities, mediated by the presence of hubs collecting data from neighboring nodes. Rakeness-based CS is used to “sample” the readings from the hubs, which, paired with a modulation of the breadth of the neighborhood from which they collect readings, allows an energy saving of more than 50% for values of the communication system parameters which are those nowadays typically employed for local (802.15.4, BLE, WiFi) and long-range transmission technologies (LoRa, GSM).
Papers [J16] and [J13] investigate the advantage of a two-step approach in the recovery of real biomedical signals acquired using CS. First, the support of the signal is computed from the CS measurements exploiting a Deep Neural Network (DNN). Once the support is known, the input signal can be easily recovered by a pseudoinverse operation. In this setting, we show that the proposed approach results in a performance improvement of more than 5 dB in terms of average reconstructed signal to noise ratio (ARSNR) compared to CS state-of-the-art approach **and allow the reconstruction of signals even when,** according to classical CS theory, **such a reconstruction should not be possible**.
Finally, Book [B1] is the first comprehensive book on CS which demonstrates that performance improvements in terms of energy saving or performance improvement in acquisition/reconstruction of a CS-based information processing system can be much larger than what is predicted by (too-loose) theoretical performance bounds. The key is (statistical) adaptation to the kind of data to acquire which is guaranteed by rakeness.
All this makes (rakeness-based-)CS truly well suited for the implementation of ultra-low-power IoT nodes.

8.3 SWITCHING POWER CONVERTERS

Timeframe: The research began immediately after the end of my PhD; it is still ongoing and growing in importance. The main collaborators are Prof. Riccardo Rovatti (Professor of Electronics since 2013 at the University of Bologna, Italy, Prof. Sergio Callegari (Former Student and Associate Professor of Electronics since 2017 at the University of Bologna, Italy), Prof. Fabio Pareschi (former student and now Associate Professor of Electronics at Politechnic of Turin), Prof. Adrian Baric (University of Zagreb, Croatia) and Dr. Giovanni Frattini (formerly with Texas Instruments, Italy; now with Analog Devices, Italy). The latter is particularly important since it reflects the industrial interest of TI and Analog Devices on this subject. Most recently, I have also initiated a collaboration with STMicroelectronics (Dr. Maria Teresa Borghi Dr. Davide Lena): STM hired two of my former students as design engineers and is financially supporting 1 new PhD. Student for the **creation of a joint STM-Politecnico di Torino laboratory** for designing Low-EMI switching power converter for automotive applications.
Rationale and contribution: The effective operation of highly-complex heterogeneous integrated circuits strongly depends upon the quality of the power delivered to the system; specifically, voltage conversion and regulation, power distribution, and power management. A comprehensive approach is not yet available for the simultaneous design of locally distributed, adaptive ultra-small on-chip point-of-load voltage regulators, decoupling capacitors, and local power controllers. In addition to the requirement of studying the effect of the complex interaction of the many on-chip point-of-load voltage regulators, power networks and power converters, there is the need to develop efficient “atomic” components (such as easily implementable switching power converters, locally intelligent power controllers, techniques for minimizing mutual converter/regulator influence in terms of Electromagnetic Interference, stability…). My contributions have been related to the latter points and, more specifically to:

- Generation of Low EMI Timing Signals for Switching Power Converters
- Improved design methodology for easily implementable of resonant converters (Class-E and LLC, also for automotive applications)

As far as the first argument is concerned, it is well known that Electromagnetic Interference (EMI) is a severe problem. For such systems, interference is mainly due to timing signals, such as clock signals, widely employed in digital circuits, or the control pulse-trains used in switching power converters. Due to their periodic nature and to the presence of sharp edges, the power of such signals is in fact concentrated at those frequencies corresponding to the multiples of the timing signal period. This can obviously produce serious problems in terms of EMI. Classical methodologies to solve this issue are costly since they require the introduction of power supply filters and metal shields.
An appreciable EMI reduction can be achieved by means of a simple quasi-stationary frequency modulation (FM) directed at intentionally perturbing a normally narrowband timing signal, thus spreading the energy associated with each harmonic over a large bandwidth in order to reduce the peak value. From this point of view, the solutions described in the literature when I started to work in this area ranged from simple sinusoidal FM to the more sophisticated case where the frequency deviation profile is expressed as a family of cubic polynomials patented by Lexmark. Notably, this last solution reduces the peak value of the spectrum by more than 7dB with respect to the unperturbed signal and has been employed in several commercial products from Intel, IBM, and Cypress.

In Paper [J76], I introduced a way to achieve lower power densities by using non-periodic modulating signals such as those coming from a 1-D chaotic map. More specifically, using SDST (see section 1) I was able to obtain a procedure that can be used to ***optimize EMI reduction in several practical applications***. In more detail, [J76] shows that:

A) the power spectral density (PSD) of an FM sinusoidal (or clock) signal modulated by a chaotic one is related to the statistical features of the chaotic signal itself, ***in any operating condition***, and
B) a simplified version of the previous relationship between the PSD and the probability density function (PDF) of chaotic samples holds ***for a modulation which is quasi stationary with respect to the carrier (slow FM)***.

The result B) is important because it offers an easy-to-use synthesis tool which computes the PDF of the chaotic samples necessary to achieve the desired PSD. More specifically, it is shown that to maximize the spectrum spread (and thus to minimize EMI) one must implement a chaotic map with uniform PDF, which offers the theoretical foundation of the practical result achieved in [J66], where practical implementation details were considered. Overall I was able to show that **chaotic modulating signals reduce the EMI spectrum by an additional 9dB with respect to the previously mentioned solutions**.
The result A) allows the extension of the spectrum shaping methodology considered for B) to any setting, and in particular for non quasi-stationary modulation which is certainly the relevant comparison to achieve a further reduction in terms of peak value in the spectrum and therefore of emitted interference.
It is worth stressing that this concept has been recognized by the community by awards and citations: [J76] is the companion paper of [J75], and together they received a total of **123 citations** according to Scopus; furthermore, Paper [J76] has also received the **IEEE CAS Society Darlington award** in 2004, and was also evaluated as **excellent** in the CIVR2001-2003 Italian research evaluation exercise.
Paper [J54] is important since it shows that the methodology can be extended also to EMI reduction in serial data communication systems. More specifically, the paper reports the design of the **first known circuits** specifically meant as a low EMI generator for 3-GHz Serial Advanced Technology Attachment II (SATA-II) applications. The circuit prototype has been implemented in 0.13 um CMOS technology and the use of chaos instead of a standard triangular modulation achieves a peak reduction greater than 14 dB measured at 100kHz RBW, **which is better than any other prototypes presented in the literature**. Furthermore, despite the fact that such an unconventional aperiodic modulating signal is used, the clock can be recovered by exploiting a standard clock and data recovery circuit at the receiver side of the SATA-II bus.
Paper [J43] and paper [J42] derive from the collaboration with Texas Instruments. Paper [J43] shows that once one takes into account the model of the EMI receiver used in the measurements (in compliance with EMC standards), the resulting effect of all modulating waveforms is different. In this paper, I and my research group dealt specifically with the case of triangular modulation and showed that **none** of the industrial products (by Cypress, TI, ON Semiconductors, Fujitsu, …) available in the market which exploit such modulation have been designed to minimize EMI if measured according to EMC standards. On the contrary, we offered a way to perform such an optimization. This is one of the paper that consider on of my key publications which was particularly impactful, as shown by the fact that it was also evaluated as **excellent** in the VQR2011-2014 Italian research evaluation exercise, and, together with the corresponding review paper [J35], received a total of **102 citations** according to Scopus.
In Paper [J42] I and my group showed that the modulating waveform able to maximize EMC can be generated by a different chaotic map (or approximated by an even simpler digital circuit) than the one used to minimize, in the ideal case studied in [J76], the peak value of the theoretical spectrum. As such, a further measured reduction of about 7dB can be obtained with respect to the use of triangular modulation. Since the above results demonstrated the advantages of the chaos-based EMI reduction technique in terms of both performance improvement and implementation cost (with respect to current technology) in a setting of clear industrial interest, it may be foreseen that this methodology **may result in a new generation of extremely low-EMI spread spectrum clock generators, and high-EMC switching power converters**, which is something that is currently under in the implementation phase by STMicrolectronics. Furthermore, this technique **can certainly be adopted for EMI reduction when multiple power supplies are needed** in the implementation of for (complex) integrated systems.

As far as the second topic is concerned, one of the natural approaches to ease integration of switching power converters is to implement resonant (Class-E) converters. They rely on the use of a resonant circuit that shapes the voltage and the current across active devices in order to synchronize the device turn-on with the zero-crossing of the voltage and the current waveforms. Reducing the voltage-current product of active devices lowers the energy-loss-per-cycle, and allows higher operating frequency, up to the VHF range (30-300 MHz). Very high switching frequency allows better transient performance and bandwidth and requires smaller passive reactive elements, thus reducing the size and cost of the converter and allowing it to be easily implemented in integrated form, even multiple times on the same chip. My main contributions in this area, **again as a result of a collaboration with TI**, are reported in [J33] [J20] and [J17]. [J33] describes an innovative analytic methodology for Class-E converter design. This method, which solves all the issues

related to the current state-of-the art design techniques (in terms of their approximation and of the consequent necessity of several time-consuming trial-and-error design attempts), provides very precise designs which very well match corresponding circuit prototype measurements. [J20] is also very important since and I and my group showed that about twenty different class-E converter architectures proposed in the last three decades can be reduced to two basic topologies, allowing the extension to all these resonant converters of the exact design procedure in [J33]. Finally, [J17] **shows how the use of the design method proposed in [J33] can lead to important breakthroughs**. In [J17], I and my group proposed a new methodology to create a through-the-barrier half-duplex bidirectional communication channel between the two sides of an isolated class-E resonant dc-dc converter. Our methodology is innovative since **communication occurs through the same transformer used for energy transfer**, and relies on connecting and disconnecting an auxiliary capacitance. By doing so, the converter switches between a faster and a slower response without any change in the clock controlling its activity and this could be achieved since the two solutions can be designed through the methodology in [J33] to be different enough to ease detection at the receiver side. With this, it is possible to achieve a very high-rate bidirectional communication (up to 1 bit per switching clock period) with virtually no limitations in the converter power with respect to a standard class-E implementation.

This activity has been overall very much appreciated by the scientific community. In addition to the already mentioned **2004 IEEE CAS Society Darlington Award** received by [J76], conference papers related to [J54], namely [C119] and [C114] received, respectively, the **best student paper award** at the International Symposium on Electromagnetic Compatibility (EMCZurich'05), and the **best paper award** at the 17th European Conference on Circuit Theory and Design (ECCTD'05). Finally, a conference paper related to [J33] and [J17], namely [C26] recently received the EMCCompo2019 **best student paper award.**

8.4 EMBEDDED SYSTEMS SECURITY

Timeframe: This research activity originated in early 2000 when I was working as an Associate Professor at the University of Ferrara and is still ongoing.
The main collaborators, belonging to my research group, are/have been Prof. Riccardo Rovatti (Professor of Electronics at the University of Bologna, Italy), Prof. Mauro Mangia (former PhD students and now Assistant Professor at the University of Bologna, Italy), Prof. Fabio Pareschi (former PhD students and now Associate Professor at the Politecnico di Torino, Italy), Prof. Sergio Callegari (former PhD students and now Associate Professor at the University of Bologna, Italy), and (Dr. Valerio Cambareri, former PhD students and now Sony Depthsensing Solutions, Belgium). I also had collaborations with Prof Kwok-Wo Wong (City University of Hong Kong, HK).

Rationale and contribution: Security is increasingly widespread in many (and perhaps all) embedded systems, ranging from the smallest RFID tag to smart cards and smart gadgets (phones, watches, …), to highly complex systems like cars or even satellites orbiting the earth. Given the future growth of data intense services expected in the coming years caused by the IoT revolution, this widespread need for security is expected to continue for many more decades. Such need is particularly pressing for embedded systems since, contrary to what has happened in other areas such as computer networking, security is here often ignored during the design and development period of the product, thus leaving many embedded devices vulnerable to attacks. This is, for instance, the case for medical devices which should be able to reliably work in body area networks; conversely, recent demonstrations of security attacks on commercial products, e.g., pacemakers and insulin pumps, have elevated medical device security from the realm of theoretical possibility to an immediate concern. Another area where security threats deserve immediate attention is the one of standard microcontrollers, for which implementing sensitive applications (such as digital locks, onetime password generators, …) can lead to severe problems.
My contributions to this problem have been in the areas of:

- Efficient random number generation for cryptography;
- Analysis of low complexity security schemes for IoT applications

One of my key contributions [J58] deals with innovative True Random Number Generators for cryptographic applications. Random Number Generators (RNGs) represent a critical point in the implementation of many security schemes and can be regarded as fundamental cryptographic primitives. For instance, random numbers are inherent in the computation of algorithms such as DSA, in the synthesis of confidential keys for symmetric- and public-key crypto-systems as RSA moduli, and in many communication protocols. The ability of cryptographic techniques to foil pattern analysis is strongly dependent on the unpredictability of the random generators they employ, so that generators suitable for security related applications must meet much stronger requirements than those for other applications. It is generally recognized that ideal (or so

called true) random number generators (TRNGs) can only be approximated. An ideal source must in fact be capable of producing infinitely long sequences made of perfectly *independent* bits, with the property that, when restarted, it never reproduces a previously delivered sequence (non-repeatability). Practical implementations of RNGs can be classified into two major categories, namely *pseudo*-RNGs and *physical*-RNGs. Pseudo-RNGs are deterministic, numeric algorithms that expand short seeds into long bit sequences. Conversely, physical-RNGs rely on microscopic processes resulting in macroscopic observables which can be regarded as random noise (quantum noise, thermal noise, etc.). Pseudo-RNGs generally depart more from the ideal specifications. Being necessarily based on finite memory algorithms, they exhibit periodic behaviors and generate correlated samples. The same reason also makes them completely repeatable and obviously *unsuitable for data security and cryptography*. Their substantial advantage is the algorithmic nature which makes them easily embeddable in any digital circuit or system. Physical-RNGs, on the other hand, are the best approximation of TRNGs. Unfortunately, they may require very specialized hardware and/or environmental conditions, which make them *expensive to embed*. In spite of this liability, security related applications have recently been strongly pushing their development and deployment, so that bigger players in IT (e.g. Intel and Via) exploited physical-RNGs in their security platforms.
Chaotic maps have always claimed to be capable of implementing TRNGs. The basic idea is that, rather than exploiting natural phenomena like noise that are hardly controllable and mathematically unmanageable, one can rely on artificial and simpler ones, as one-dimensional chaotic maps, that derive unpredictability from complexity.
My main contributions in this field have been to tackle this problem **both at the theoretical and system design level**. By exploiting SDST, I have introduced in [J58] a novel methodology for the implementation of TRNGs which ***closes the gap with the processing speed and ease of implementation of pseudo-RNGs***. More specifically, I have been able to analytically ***prove*** that chaotic maps exist that behave as TRNGs in an ideal setting and that robustly maintain such properties with respect to implementation errors, and, furthermore, that such maps ***can be practically realized out of pipeline analog-to-digital converters (ADC) parts*** which are now ubiquitous in any mixed mode system. With this, one can easily reuse design expertise and even analog Intellectual-Property (IP) blocks **to quickly embed true random sources in SOCs and specialized apparatuses**. It is also noted that this paper was evaluated as **excellent** in the Italian research evaluation exercise VQR2004-2010 and receive overall **193 citations** according to Scopus.
Paper [J53] describes the implementation of a chaos-based TRNG based on this approach in AMS 0.35um CMOS technology and in UMC 0.18um CMOS technology. Here my role has been that of co-designer of the chip and I dealt with the interpretation of the statistical tests necessary to evaluate performance. Measurement results showed that the designed chaos-based TRNGs:

- operate at a bitrate of approximately 40Mbits/s and 100Mbits/s, namely ***10 to 100 times faster*** than current state-of-the-art TRNGs, such as the Physical-RNG proposed by Intel or other commercial solutions proposed by VIA (Padlock) and idQuantique (Quantis);
- behave in ***a completely satisfactory way*** when validated against two standard randomness test suites proposed by NIST (FIPS 140.2 and SP800-22) and also against an enhanced version that we have proposed [J40].

Both the above mentioned contributions have been very impactful. In fact, [J53] has received **176 citations** according to Scopus (including the 63 received by [C102] of which it is the follow-up), while [J49] received **134 citations** (including the 35 received by [C86] of which it is the follow-up) and was evaluated as **excellent** in the Italian research evaluation exercise VQR2011-2014.

As far as the analysis of low-complexity security schemes are concerned, in the two companion papers [J41] and [J36], I was able to exploit CS for **achieving data privacy at zero-cost**. More specifically, I devised a data hiding strategy which relies on the fact that any user decoding the CS measurements must be completely aware of the sampling sequences used in the acquisition process in order to achieve exact reconstruction. In the absence of this information, the recovered signal will be subject to reconstruction noise so large as to make it substantially unusable. I have been able to quantify the trade-off between uncertainty in the CS sampling sequences and quality of the reconstructed signal, thereby quantifying the trade-off between security properties and resource requirements. This paves the way to use CS for **an almost-zero cost data hiding mechanism in low-complexity systems such as IoT nodes,** for which the use of standard cryptography is not an option. Furthermore, paper [J20] builds on the results of [J41] and [J36] to evaluate the impact on security of adoption of rakeness-based CS during the acquisition phase. Results shows that, especially for Known Plaintext Attacks, there is a trade-off between the compression performance (which is improved with rakeness-based CS) and obtained security. Yet, even when compression is significantly increased with respect to classical CS, the computational resources needed by an attacker to reveal the original signal appear to be well beyond what can be reasonably spent to obtain protected information with limited value, like most sensor acquisitions are. As such, rakeness-based CS can be used for performance improvements in data acquisition when limited resources are available like in the **implementation of secure ultra-low power IoT nodes.**

8.5 INFORMATION PROCESSING IN ARTIFICIAL NEURAL NETWORKS

Timeframe: The research was carried out mainly during my Ph.D. and particularly during the visit to the Laboratory of Nonlinear Systems (LANOS) at EPFL (1994-1995). The main collaborators are Prof. Patrick Thiran (EPFL, Switzerland), Prof. Martin Hasler (EPFL, Lausanne, now retired), Prof. L. O. Chua (UC Berkeley, USA, now retired).

Rationale and contribution: The main subject of study are locally coupled recurrent networks know as Cellular Neural Networks (CNNs), introduced by L. O. Chua in 1988. Their interest lies in the ease of their implementation. Their main application field is fast preprocessing of signals, particularly images. At the time I started to work in this area, although some interesting applications had already been shown, the problem of design of the CNN weights to achieve a desired operation was still unsolved. Similarly, the potential of CNNs for information processing was just emerging.
The difficulty of this research arises from the fact that a CNN is a high-dimensional non-linear dynamical system, but the regular structure of the network can be sometimes conveniently exploited.
Such exploitation is exactly what happened in [J96] and [J97], where I obtained the first significant results on the dynamics of information propagation in the simplest nontrivial CNN, which is one-dimensional and has connections between nearest neighbours. I have shown that two behaviours are possible: local diffusion (LD) of information between neighbouring cells and global propagation (GP) through the entire array. Roughly speaking, we can say that a CNN behaves in a local diffusion mode when two distant cells do not influence each other, if the states of a number r of adjacent cells located between these two cells have reached some value. Otherwise, it behaves in a global propagation mode, i.e., when one of these two cells can always influence the other one, whatever the value of the state of r adjacent cells located in between these two cells. Hence, a CNN working in the local diffusion mode operates in a very parallel way, thereby keeping its fast processing speed even for large arrays. Conversely, in a CNN operating in GP mode, the state of any cell influences the state on any other cells, so that the network processes the information in a truly global way, but with a speed that grows more than linearly with the number of nodes. Such a distinction also has important consequences on the dynamical and steady-state behavior. More specifically, I was able to show that:

- a CNN operating in LD mode possesses equilibrium points only, while in GP mode periodic steady state solutions are also possible;
- the number of steady state solutions grows exponentially with the number of cells for a LD CNN and at most linearly for a GP CNN.

As a last remark, it is worthwhile to note that several of the CNN modes of operation fall in these two classes.
In [J100] I have been able to show some interesting properties of pattern formations with CNNs. The most interesting results that have been achieved are related to the capacity of CNNs to mimic mammalian coat patterns employing a simple model with respect to classical reaction-diffusion mechanisms. Important by-products of this study have been some of the first analytical results on the relationships between CNNs' mode of operation and systems of partial differential equations.

9. Teaching Activity

9.1 SUPERVISION/MENTORSHIP AND OTHER ACTIVITY RELATED TO TEACHING

Since 1997 I have supervised a research group working in the area of nonlinear dynamics and signal processing, from theory to application to several information technology problems. The research group is strongly multidisciplinary with interests ranging from optimization of DS-CDMA communication, EMI reduction in digital and switching power converters, random number generation in cryptography and security, biomedical circuits, systems and signal processing, to, most recently, improved compressive sensing acquisition algorithms and analog-to-information converter implementation, as well as improved methodology for the design of resonant switching power converters.
In this framework I have (co)supervised or am currently (co)supervising **the activity of 36 young scientists**, 26 as PhD students and 14 as research fellows/Post-Doc (6 of them had both roles) and 2 as Research Scientist (among which five have tenure or tenure-track position) as reported in the following table.

Name	Roles when advised by me	Years	Current Position
Dr. Akim Gazali	Research Scientist	2023-	Research Scientist, KAUST, KSA
Dr. Selma Amara	Research Scientist	2023-	Research Scientist, KAUST, KSA
Dr. Charalampos Antoniaidis	Post-Doc	2023-	Post-Doc, KAUST. KSA
Mr. Mohammed Alwagait	Ph.D. Student	2024-2028	Ph.D. Student, KAUST, KSA
Mrs. Elham Binshaflout	Ph.D. Student	2023-2026	Ph.D. Student, KAUST, KSA
Mr. Aijaz Lone	Ph.D. Student	2023-2025	Ph.D. Student, KAUST, KSA
Mrs. Elisabetta Spinazzola	Research Fellow (Assegnista di Ricerca)	2023-2024	Reserach Fellow, Politecnico di Torino, IT
Mrs. Silvia Simone	Ph.D. Student	2021-2024	Ph.D. Student, Politecnico di Torino, IT
Mrs. Chiara Boretti	Ph.D. Student	2021-2024	Ph.D. Student, Politecnico di Torino, IT
Mr. Philippe Bich	Ph.D. Student	2021-2024	Ph.D. Student, Politecnico di Torino, IT
Mr. Francesco Gabriele	Ph.D. Student	2021-2024	Ph.D. Student, Politecnico di Torino, IT
Mr. Andrea Celentano	Research Fellow (Borsista di Ricerca) Ph.D. Student	2019-2023	Ph.D. Student, Politecnico di Torino, IT
Dr. Luciano Prono	Ph.D. Student	2019-2022	Assistant Professor, Politecnico di Torino, IT
Dr. Carmine Paolino	Ph.D. Student	2019-2022	Post-Doc, Tufts University, Boston, USA
Dr. Alex Marchioni	Ph.D. Student	2018-2021	Assistant Professor, University of Bologna, IT
Dr. Hugo Pimentel	Ph.D. Student	2016-2019	Software Engineer, ARCA Tecnologie srl, Imola, IT
Dr. Nicola Bertoni	PhD Student	2014-2016	Power Circuit Engineer, Texas Instruments, Frising, DE
Dr. Valerio Cambareri	PhD Student	2012-2014	Senior System Engineer (R&D), Sony Depthsensing Solutions SA, Brussels, B
Dr. Carlos Formigli	PhD Student	2011-2013	Research Associate, National University of Tucuman, Argentina

Dr. Javier Haboba	PhD Student	2011-2013	Product Manager / Head of Hardware at Maxeler Technologies, London, UK
Dr. Salvatore Caporale	Post-Doctoral Research Fellow (Assegnista di Ricerca)	2010-2015	Technologist, Cirrus Logic, Edinburgh, UK
Dr. Mauro Mangia	PhD Student Post-Doctoral Research Fellow (Assegnista di Ricerca)	2010-2012 2013-2016	Assistant Professor, University of Bologna, IT
Dr. Ludovico Ausiello	PhD Student	2005-2008	Acoustic Engineer at Tannoy, Coatbridge, UK
Mr. Marco Bassani	Research Fellow	2005-2006	Digital Hardware Designer at Datalogic Automation, Bologna, IT
Mr. Mattias Ballardini	Research Fellow	2005-2006	Systems Architect at SACMI, Imola, IT
Dr. Giampaolo Cimatti	Research Fellow	2005-2006	Head of Small Wind Power Business Unit, Tozzi Nord, Ravenna, IT
Dr. Luca Antonio De Michele	PhD Student	2004-2006	Equipment Testing and Maintenance Expert, Allstom, Bologna, IT
Dr. Fabio Pareschi	PhD Student Post-Doctoral Research Fellow (Assegnista di Ricerca)	2004-2006 2007-2013	Associate Professor, Politecnico di Torino, IT
Dr. Marco Lazzarini	Research Fellow	2004	System Engineer, Bluecardio SRL, Ferrara, IT
Dr. Stefano Vitali	PhD Student Post-Doctoral Research Fellow (Assegnista di Ricerca)	2003-2005 2006-2007	Senior Design Engineer, Digital Systems & Signal Processing, eWings s.r.l, Bologna, IT
Dr. Federico Agnelli	PhD Student	2003-2005	CEO, Deltacommerce s.r.l., Ferrara, IT
Dr. Marco Cisterni	Research Fellow	2002	System Engineer, Marposs s.p.a., Bologna, IT
Dr. Stefano Santi	PhD Student	2002-2004	Image Processing Algorithm Developer, Datalogic, Bologna, IT
Dr. Michele Balestra	PhD Student Post-Doctoral Research Fellow (Assegnista di Ricerca)	2000-2002 2003-2008	Software Engineer and Web Designer, Lepida SpA, Bologna, IT
Dr. Sergio Callegari	PhD Student Post-Doctoral Research Fellow (Assegnista di Ricerca)	1997-1999 2000-2002	Associate Professor, University of Bologna, IT

Overall I have (co)supervised over 100 (5Y-)Laurea degree/Bachelor/Master thesis projects, the vast majority at master level and some in cooperation with leading Microlectronic industries like TI, Analog Devices and STMicrolectronics. A partial list of the students and institution is reported below, excluding those that were already mentioned as Master Students in the table above:

Adriana Telesca, (UNIFE); Alessandro Urso, (UNIFE); Alex Sintoni, (UNIFE); Barbara Beccati, (UNIFE); Biondi Luca, (UNIFE); Carlo Abosinetti, (UNIBO); Claudio Bacchiani, (UNIBO); Claudio Giordani, (UNIBO); Cristiano Querzè, (UNIFE); Damiano Casari, (UNIBO); Daniele Loreto, (UNIBO); Dario Zaccarini, (UNIBO); Davide di Nunzio, (UNIBO); Davide Salviani, (UNIBO); Davide Vergnani, (UNIFE); Denny Tieghi, (UNIFE); Domenico Savastano, (UNIFE); Ercole Esposito, (UNIBO); Fabio Boscolo, (UNIFE); Fabio Garzia, (UNIBO); Fabrizio Boarini, (UNIFE); Fabrizio Viara, (UNIFE); Federico Natali, (UNIBO); Francesco Bartoli, (UNIBO);

Francesco Brandoli, (UNIBO); Francesco Tomesani, (UNIBO); Gaeatno Bullone, (UNIFE); Galuppi Andrea, (UNIFE); Gianluca Berghella, (UNIBO); Gianluca Grandi, (UNIBO); Gianni Veneselli, (UNIBO); Giorgio Greco, (UNIFE); Giovanni Gallini, (UNIFE); Giovanni Marchi, (UNIBO); Giovanni Maria Maccioni, (UNIBO); Luca Covino, (UNIBO); Luciana Carota, (UNIBO); Lucio Madella Amadei, (UNIBO); Marco Bassani, (UNIBO); Marco Ghetti, (UNIBO); Marco Liverani, (UNIBO); Marco Simonetti, (UNIBO); Matias Ballardini, (UNIBO); Matteo Mantovani, (UNIFE); Maurizio Paggini, (UNIBO); Maurizio Tomassetti, (UNIFE); Nicola Alessi, (UNIBO); Padovani Claudio, (UNIFE); Paluan Luca, (UNIFE); Paolo Capati, (UNIFE); Pasqualino Costa, (UNIBO); Piergiorgio Sordo, (UNIFE); Riccardo Bevilacqua, (UNIFE); Saverio di Pompeo, (UNIBO); Simone Gagliano, (UNIBO); Simone Giorgi, (UNIFE); Simone Pretti, (UNIFE); Stefano Toselli, (UNIFE); Tommaso Autiero, (UNIBO); Valerio Cambareri, (UNIBO); Letizai Magenta (UNIBO); Fabio Bertini, (POLITO); Fabrizio Congia, (POLITO); Riccardo Masera, (POLITO); Stefano Panaro, (POLITO); Cristian Mastronardi, (POLITO); Giovanni Masci, (POLITO); Giovanni Giorgino, (POLITO); Arrivabeni Luana, (POLITO); Stefano Panaro, (POLITO); Alice Vagnone, (POLITO); Vastato Salvatore, (POLITO); Trobiani Valerio, (POLITO); Manello Simone, (POLITO); Francesco Gabriele, (POLITO); Chiara Boretti, (POLITO); Philippe Bich, (POLITO); Domenico Salime, (POLITO); Silvia Simone, (POLITO); Francesco Trinca, (POLITO);

It is noteworthy that in several cases the special projects of undergraduate/master students whom I supervised led to publications, highlighting my commitment to offering research experiences to all students: I consider a research project a *seminal opportunity* to transition a student from the *passive role* of an individual sitting in a classroom to that of an *active professional responsible for understanding and advancing the state of knowledge in the field*. The list is these special project topics is reported below (see also full list of publications).

Student Name	Project Topic (Master's/Bachelor's/Semester Project)	Published Work	Current Position
Andrea Celentano	A Resonant Class-E DC-DC converter for Wireless Power Transfer in implantable Stimulators	[C17]	PhD Candidate, Politecnico di Torino, IT
Carmine Paolino	Compressed Sensing Architecture based on a SAR ADCs (Master's degree project) **Recipient of the PRIME2019 best student paper award** (Gold Leaf)	[C21]	PhD Candidate, Politecnico di Torino, IT
Luciano Prono	A framework for non-recurrent artificial neural networks implementation on FPGA (Master's degree project)	[C22]	PhD Candidate, Politecnico di Torino, IT
Letizia Magenta	Improved Disturbance Rejection in Rakeness-Based Compressed Sensing (Master's degree project)	[C27]	
Tommaso Vincenzi	EMI reduction in Class-E Resonant Switching Power Converters (Semester project)	[C41]	PhD candidate, ETH Zurich, CH
Stefano Bocchi	Ripple-based communication over a DC-bus (Master's degree project)	[C44]	eWings SRL, Bologna, IT
Nicola Bertoni	Class-E resonant converter design (Master's degree project)	[C45] [C46]	PhD Student, University of Ferrara, IT
Nicola Bertoni	Decoding algorithms for Compressed Sensing (semester project)	[C56]	PhD Student, University of Ferrara, IT
Mauro Mangia	Compressive sensing based on rakeness (Master's degree project) recipient of the **ICAS2011 best student paper award** and of the **2013 IEEE CAS Society Guellemin-Cauer Award**;	[C69] [J46]	Assistant Professor, University of Bologna, IT
Mauro Mangia	Narrowband interference cancellation in UWB	[C75]	Assistant Professor,

	communication based on chaos (Semester project)	[J48]	University of Bologna, IT
Juri Ranieri	Compressed sensing based on rakeness (Master's degree project)	[C74]	Google, Zurich, CH
Giampaolo Cimatti	Chaos-based UWB communication in WSNs (Master's degree project)	[C98] [J59]	Head of Small Wind Power Business Unit, Tozzi Nord, Ravenna, IT
Luca Antonio De Michele	EMI reduction via chaos-based spread spectrum clocking (Master's degree project) recipient of the **EMCZurich2002 best student paper award**;	[C113]	Equipment Testing and Maintenance Expert, Allstom, Bologna, IT
Stefano Poli	Post-processing techniques for high-throughput TRNGs (Semester project)	[C120]	Spice Modeling Specialist at Texas Instruments, Dallas, USA
Federico Agnelli	Implementation of a prototype of a Chaos-based DS-CDMA communication systems (Master's degree project)	[C154] [C158]	CEO, Deltacommerce s.r.l., Ferrara, IT
Marco Cisterni	Computation of PSD of randomly jittered PWM signals (Bachelor's degree project)	[C126]	System Engineer, Marposs s.p.a., Bologna, IT
Stefano Santi	Zero-crossing statistics of chaos-based FM clock signals (Master's degree project)	[C133] [J72]	Image Processing Algorithm Developer, Datalogic, Bologna, IT
Mirko Dondini	Adaptive threshold in post-processing techniques for high-throughput TRNGs (Master's degree project)	[C159]	
Andrea Cesaroni	Design of a mixed-mode TRNGs (Master's degree project)	[C156]	
Michele Balestra	Prototype implementation of a chaos-based spread-spectrum clock generator with off-the-shelves components (Master's degree project)	[C172]	Software Engineer and Web Designer, Lepida SpA, Bologna, IT
Luca Ravezzi	Design and implementation of a current-mode Cellular Neural Network (Master's degree project)	[C195] [J81]	Distinguished Engineer at Applied Micro, San Francisco, USA
Sergio Callegari	Design of a CMOS chaotic tailed tent-map for robust random number generation (Master's degree project)	[C201]	Associate Professor, University of Bologna, IT

In addition, I have contributed to doctoral education internationally by directing a Ph.D. program on Information Technology at the European level (European Doctorate in Information Technology – EDITH). I served as the PI for this program – specifically, I wrote the proposal and oversaw its implementation. Funds for the project came from the European Commission (EC) in the framework of the "Marie Curie" program[5]. The EDITH project received approximately €2M after an extremely competitive selection phase (7% success rate for 750 proposal submissions).

The aim of the program was to establish a doctoral training program for students coming mainly from (but not limited to) European countries in highly qualified European Universities and Research Centers working in the fields of Information Technology (IT). The objectives of the Doctorate program may be summarized as follows:

1. To *broaden* the spectrum and the breath of competence of young researchers in the field of IT;

[5] The "Marie Curie" initiative is a program financed by the EC to allow mobility of young (less than 4 years of research experience) as well as experienced (more than 4 years and less than 10 years of research experience) researchers across all of Europe. More details can be found at http://http://europa.eu.int/comm/research/fp6/mariecurie-actions/indexhtm_en.html

2. To give them *research skills* necessary to obtain specialist knowledge of subjects pertinent to IT;
3. To provide them the ability to use *logical and lateral thinking* needed to achieve creative and innovative solutions to engineering problems;
4. To *bring together* the unique *teaching* and *research* features of highly qualified European University and Research Centers with complementary expertise working in the fields of Electronics, Information and Communication Technologies;
5. To create a *link* between *academic* and *industrial* bodies in Europe.

The EDITH consortium[6] had very broad training capabilities in all fields related to IT, starting from microelectronics manufacturing process and materials (DUT, CEA-LETI, IMEC), to device modeling and characterization (UB-ARCES, INPG) and circuit and systems design (UB-ARCES, DUT, K.U.Leuven), and from signal processing, wireless and computer communication, and ad-hoc networks (UB-ARCES, EPFL-I&C, INPG) to high level applications (UB-ARCES, EPFL-I&C). Exploiting the research and teaching excellence in the above fields in a fully synergetic way, the members of EDITH consortium offered young researchers a unique opportunity to achieve both:

- a horizontal training in several topics related to IT, by means of short- and medium-term visits in one or more consortium partner institutions;
- a deep vertical preparation in a given domain of interest for the student, by performing the largest part of the training in the most qualified partner institution.

Besides the training by research, we developed a series of short Ph.D. courses offered to the students in the most qualified Institution of the EDITH consortium.

This Ph.D. program was also complemented by the Internationalization project “Applications of Nonlinear Dynamics to Information Technology,” which was financed by Italian MIUR. This project involved the following research institutions:

1. Queen Mary University of London, UK
2. Swiss Federal Institute of Technology in Lausanne (EPFL), CH
3. IBM, T. J. Watson Research Laboratories, US
4. University of California San Diego (UCSD), US
5. Northeastern University, Boston, US
6. STMicroelectronics, Wireless Research Center, Geneva, CH
7. University of Washington, Seattle, USA
8. City University, Hong Kong
9. Polytechnic University, Hong Kong

The aim of the project was to finance the mobility of staff members and Ph.D. students belonging to all institutions and offer them the chance to further strengthen the ongoing research cooperation in the field of application of nonlinear dynamics to IT.

9.2 TEACHING EXPERIENCE

Each year since 1996, I have been teaching Bachelor’s and/or Master’s degree courses, as well as those for the old regulation “five-year (5Y-)Laurea degree”[7]
The list of courses is reported below and the list of the topics for each class is reported at the end of the section.
All classes have been taught in Italian apart from “Circuits and Algorithms for Statistical Signal Processing” for the AY 2015/2016 and “Analog Integrated Circuits” from AY 2017/2018 to 2019/2020 which have been taught in English.

- **AY 1996/97** (responsibility given according to art. 100 D. P .R. 382/80)
    1. Electronics III (Elettronica III), 5Y-Laurea degree in Electronic Engineering, Faculty of Engineering, University of Ferrara [6h (theory per week) + 2h (exercises per week)].

[6] See page 42 for the consortium members

[7] The only exceptions are during the Academic Year (AY) 1998/99, since the formal responsibility of a course was not possible for me as it was incompatible with respect to my newly assumed position of Assistant Professor (Ricercatore non Confermato) at the Department of Engineering of the University of Ferrara (cfr. art. 100 D.P.R. 382/80). I am also not teaching since I assumed the role of Dean at KAUST in October 2022.

- **AY 1997/98** (responsibility given according to art. 100 D. P .R. 382/80)
    1. Electronics III (Elettronica III), 5Y-Laurea degree in Electronic Engineering, Faculty of Engineering, University of Ferrara [6h (theory per week) + 2h (exercises per week)].
- **AY 1999/2000**
    1. Architectures of Analog Integrated Circuits and Systems, 5Y-Laurea degree in Electronic Engineering, Faculty of Engineering, University of Ferrara [6h (theory per week) + 2h (exercises per week)].
- **AY 2000/2001**
    1. Architectures of Analog Integrated Circuits and Systems, 5Y-Laurea degree in Electronic Engineering, Faculty of Engineering, University of Ferrara [6h (theory per week) + 2h (exercises per week)].
    2. Circuit Theory, 5Y-Laurea degree in Electronic Engineering, Faculty of Engineering, University of Ferrara [6h (theory per week) + 2h (exercises per week)].
- **AY 2001/2002**
    1. Architectures of Analog Integrated Circuits and Systems, 5Y-Laurea degree in Electronic Engineering, Faculty of Engineering, University of Ferrara [6h (theory per week) + 2h (exercises per week)].
    2. Circuit Theory, Bachelor's degree in Electronic and Telecommunication Engineering, Bachelor's degree in Informatics Engineering, Bachelor's degree in Automation Engineering Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
- **AY 2002/2003 [18 Credits (CFU)]**
    1. Architectures of Analog Integrated Circuits and Systems, 5Y-Laurea degree in Electronic Engineering, Faculty of Engineering, University of Ferrara [6h (theory per week) + 2h (exercises per week)].
    2. Analog Circuits for Signal Processing, Master's degree in Electronic Engineering, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
    3. Circuit Theory, Bachelor's degree in Electronic and Telecommunication Engineering, Bachelor's degree in Informatics Engineering, Bachelor's degree in Automation Engineering Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
- **AY 2003/2004 [12 Credits (CFU)]**
    1. Circuits and Algorithms for Statistical Signal Processing, Master's degree in Engineering and Technology for Electronics and Telecommunication, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
    2. Circuit Theory, Bachelor's degree in Electronic and Telecommunication Engineering, Bachelor's degree in Informatics and Automation Engineering, University of Ferrara [6 Credits (CFU)].
- **AY 2004/2005 [12 Credits (CFU)]**
    1. Analog Circuits for Signal Processing, Master's degree in Engineering and Technology for Electronics and Telecommunication, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
    2. Circuit Theory, Bachelor's degree in Electronic and Telecommunication Engineering, Bachelor's degree in Informatics and Automation Engineering, University of Ferrara [6 Credits (CFU)].
- **AY 2005/2006 [12 Credits (CFU)]**
    1. Circuits and Algorithms for Statistical Signal Processing, Master's degree in Engineering and Technology for Electronics and Telecommunication, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
    2. Circuit Theory, Bachelor's degree in Electronic and Telecommunication Engineering, Bachelor's degree in Informatics and Automation Engineering, University of Ferrara [6 Credits (CFU)].
- **AY 2006/2007 [12 Credits (CFU)]**
    1. Analog Circuits for Signal Processing, Master's degree in Engineering and Technology for Electronics and Telecommunication, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
    2. Circuit Theory, Bachelor's degree in Electronic and Telecommunication Engineering, Bachelor's degree in Informatics and Automation Engineering, University of Ferrara [6 Credits (CFU)].
- **AY 2007/2008 [12 Credits (CFU)]**

1. Circuits and Algorithms for Statistical Signal Processing, Master's degree in Engineering and Technology for Electronics and Telecommunication, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
2. Circuit Theory, Bachelor's degree in Electronic and Telecommunication Engineering, Bachelor's degree in Informatics and Automation Engineering, University of Ferrara [6 Credits (CFU)].

- **AY 2008/2009 [12 Credits (CFU)]**
  1. Analog Circuits for Signal Processing, Master's degree in Engineering and Technology for Electronics and Telecommunication, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
  2. Circuit Theory, Bachelor's degree in Electronic and Telecommunication Engineering, Bachelor's degree in Informatics and Automation Engineering, University of Ferrara [6 Credits (CFU)].
- **AY 2009/2010 [6 Credits (CFU)]**
  1. Circuits and Algorithms for Statistical Signal Processing, Master's degree in Electronic and Telecommunication Engineering, Faculty of Engineering, University of Ferrara [6 Credits (CFU)]. During this year I taught only one class due to the shift of Circuit Theory from the first to the second year of the Bachelor's degree in Electronic and Telecommunication Engineering.
- **AY 2010/2011 [15 Credits (CFU)]**
  1. Analog Circuits for Signal Processing, Master's degree in Electronic and Telecommunication Engineering, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
  2. Circuit Theory, Bachelor's degree in Information Engineering, University of Ferrara [9 Credits (CFU)].
- **AY 2011/2012 [15 Credits (CFU)]**
  1. Circuits and Algorithms for Statistical Signal Processing, Master's degree in Electronic and Telecommunication Engineering, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
  2. Circuit Theory, Bachelor's degree in Information Engineering, University of Ferrara [9 Credits (CFU)].
- **AY 2012/2013 [15 Credits (CFU)]**
  1. Analog Circuits for Signal Processing, Master's degree in Electronic and Telecommunication Engineering, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
  2. Circuit Theory, Bachelor's degree in Information Engineering, University of Ferrara [9 Credits (CFU)].
- **AY 2013/2014 [15 Credits (CFU)]**
  1. Circuits and Algorithms for Statistical Signal Processing, Master's degree in Electronic and Telecommunication Engineering, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
  2. Circuit Theory, Bachelor's degree in Information Engineering, University of Ferrara [9 Credits (CFU)].

- **AY 2014/2015 [15 Credits (CFU)]**
  1. Analog Circuits for Signal Processing, Master's degree in Electronic and Telecommunication Engineering, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
  2. Circuit Theory, Bachelor's degree in Information Engineering, University of Ferrara [9 Credits (CFU)].
- **AY 2015/2016 [15 Credits (CFU)]**
  1. Circuits and Algorithms for Statistical Signal Processing, Master's degree in Electronic and Telecommunication Engineering, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
  2. Circuit Theory, Bachelor's degree in Information Engineering, University of Ferrara [9 Credits (CFU)].
- **AY 2016/2017 [15 Credits (CFU)]**
  1. Analog Circuits for Signal Processing, Master's degree in Electronic and Telecommunication Engineering, Faculty of Engineering, University of Ferrara [6 Credits (CFU)].
  2. Circuit Theory, Bachelor's degree in Information Engineering, University of Ferrara [9 Credits (CFU)].
- **AY 2017/2018 [21 Credits (CFU)]**
  1. Circuit Theory, Bachelor's degree in Electronic and Computer Engineering, Faculty of Engineering, University of Ferrara [9 Credits (CFU)].

2. Electronics Systems, Technologies and Measurements, Bachelor's degree in Computer Engineering, Politecnico di Torino [6 Credits (CFU) – 4CFU taught by a colleague].
3. Analog Integrated Circuits, Master's degree in Electronic Engineering, Politecnico di Torino [6 Credits (CFU)].

- **AY 2018/2019 [16 Credits (CFU)]**
  1. Applied Electronics, Bachelor's degree in Engineering Physics, Politecnico di Torino [10 Credits (CFU)].
  2. Analog Integrated Circuits, Master's degree in Electronic Engineering, Politecnico di Torino [6 Credits (CFU)].
- **AY 2019/2020 [16 Credits (CFU)]**
  1. Applied Electronics, Bachelor's degree in Engineering Physics, Politecnico di Torino [10 Credits (CFU)].
  2. Analog Integrated Circuits, Master's degree in Electronic Engineering, Politecnico di Torino [6 Credits (CFU)].
- **AY 2020/2021 [16 Credits (CFU)]**
  1. Applied Electronics, Bachelor's degree in Engineering Physics, Politecnico di Torino [10 Credits (CFU)]. The class **has been flipped** to take advantage of remote learning during Covid. All material provided to students (in Italian) can be fount at https://www.dropbox.com/sh/6aotsx8uaz0xff4/AABDu3F9BGgSsUXcoP0SYU6Ba?dl=0
  2. Analog Integrated Circuits, Master's degree in Electronic Engineering, Politecnico di Torino [6 Credits (CFU)].
- **AY 2021/2022 [16 Credits (CFU)]**
  1. Applied Electronics, Bachelor's degree in Engineering Physics, Politecnico di Torino [10 Credits (CFU)].
  2. Analog Integrated Circuits, Master's degree in Electronic Engineering, Politecnico di Torino [6 Credits (CFU)].
- **AY 2022/2023 [16 Credits (CFU)]**
  1. Applied Electronics, Bachelor's degree in Engineering Physics, Politecnico di Torino [10 Credits (CFU)].
  2. Analog Integrated Circuits, Master's degree in Electronic Engineering, Politecnico di Torino [6 Credits (CFU)].

Circuit Theory, mandatory course for 2nd year students of a 3-year Bachelor Program in Electronic Engineering and Computer Science. The goal of the course is to provide the students with the basic concepts in electrical phenomena.

The topics covered in this course are: introduction to electrical engineering; basic circuit and systems concepts; mathematical models of components; Kirchhoff's laws; resistors, sources, capacitors, inductors, operational amplifiers, piecewise nonlinear resistors, transformers, gyrators; solution of first and second order linear differential equations associated with basic circuit forms; transient analysis and Laplace transform, steady state sinusoidal excitation, phasors, system functions, and complex frequency; frequency response; computer analysis of electrical circuits; power and energy; two-port network theory.

Analog Circuits for Signal Processing, mandatory graduate course for 1st year students of a 2-year Master's program in Electronic and Telecommunication Engineering. The goal of the course is to provide students with basic and advanced concepts in CMOS Analog Integrated Circuits design.

The topics covered in this course are: MOS operation (weak, moderate, strong inversion); basic transistor stages with low voltage supplies; basic MOS amplifiers (common source, common drain, common gate, cascade) and their frequency response; building blocks of analog integrated circuits: current sources and mirrors, level shifters, and output stages; differential amplifier circuit; introduction to operational amplifier circuits; study of operational amplifier design techniques involving current mirrors and active loads (telescopic, folded cascode, two-stage OTA, two-stage cascode OTA); stability and frequency compensation techniques; design and analysis of active filters; switched capacitor amplifier and filter: time-domain settling; switch design and non-idealities; CAD tools for circuit design.

Circuits and Systems for Statistical Signal Processing, elective graduate course for 2nd year students of a 2-year Master's Program in Electronic and Telecommunication Engineering. This course focuses on

statistical estimation and characterization of signals, as well as on the analysis of the stochastic processes that model or are generated by some artificial dynamical systems or electronic circuits.

The topics covered in this course are: random variables and stochastic processes and their characterization (σ-algebra and probability, probability density and distribution, expected value, moments and covariance, characterization of stochastic process by joint probabilities, correlations and projections); stationary, ergodic, mixing and exact processes; static transformations (transformation with a finite number of counterimages, linear transformation, quantization); linear filtering (characterization with joint probabilities, correlations and projections, ideal low-pass filters); random variables and Gaussian processes (real and complex Gaussian random vectors, Gaussian stochastic processes, Gaussian white noise); power density spectrum (energy and power spectrum, Wiener-Khinchin theorem, power spectrum estimation: periodogram and minimum variance methods); linear prediction (linear prediction and orthogonality principle, regular and predictable stochastic process, Wold decomposition); self-similar processes (asymptotic second-order self-similarity, self-similarity and autocorrelation profile, self-similarity and 1/f spectrum); finite memory processes (definitions, memory 1 stochastic processes, link with dynamical systems); piecewise affine Markov maps and relationships with Markov chains; applications to DS-CDMA performance optimization, EMI reduction, artificial self-similar traffic generation, random number generation.

Analog Integrated Circuits, elective graduate course for 2nd year students of a 2-year Master's program in Electronic Engineering. The goal of the course is to teach students the various steps necessary to design and implement the most common analog circuits (op-amps, filters, switched capacitor circuits…). CMOS technology features and circuits presented in the previews courses are reviewed, and then suitably modified/enhanced to improve the likelihood to be seamlessly implemented in an integrated circuit. The most popular solutions are first analyzed with a "pencil and paper" approach in class and then fully designed using advanced CAD tools (Cadence) in the labs.

The topics covered in this course are: Basic analog cells; Review on CMOS technology, active and passive device models; fabrication tolerances and device mismatch; Nwell, metal, active, poly and select layers; Bias circuits. Voltage and current reference; Folded-cascode and Miller operational transconductance amplifiers (OTAs); Output stages; Fully differential OTAs. Common mode feedback; Discrete-time signal processing fundamentals: sampling and z-transform; Design of digital filters; Switched-capacitor circuits and filters.

Electronics Systems, Technologies and Measurements, mandatory course for 3rd year students of a 3-year Bachelor program in Computer Engineering. The goal of the course is to provide students the general characteristics of an analog, digital or hybrid electronic system. The main analysis methods, implementation choices and fabrication technologies are presented. The course in particular is devoted to the study of some fundamental electronic modules like amplifiers realized with operational amplifiers in feedback configuration, interface stages and basic logic circuits, and analyzes the operation of the most important electronic devices.

The topics covered in this course are: Introduction to electronic systems; functional module decomposition of a complex electronic system, time- and frequency-domain signal representation, analog and digital signals; amplifier classification and main parameters; negative feedback operational amplifiers. Inverting and non-inverting amplifiers, also with reactive elements and with several inputs; real operational amplifiers; open loop amplification, input differential resistance, output resistance; input currents and input offset voltage; trans-characteristics and limitations; frequency response, slew-rate and stability; threshold comparators: circuits and applications; Hysteresis voltage comparators; Square-wave and triangular waveform generators.

Applied Electronics, mandatory course for 3rd year students of a 3-year Bachelor program in Physics Engineering. The goal of the course is to provide students the capability to design circuits that are the basis of today's analog and digital electronic systems. Real operational amplifiers are first introduced and used to perform linear and non-linear functions. The class then move on to the study of the stability of circuits and quasi-sinusoidal oscillators and relaxation. The study of chaotic behavior in continuous-time and discrete-time electronic circuits is finally introduced.

The topics covered in this course are: structure of BJT and MOS operational amplifiers: current mirror, differential stage, power output stage; non-ideal parameters of operational amplifiers, frequency response, stability; linear circuits: amplifier, adder, instrumentation amplifier; active filters: first order, second order, higher order; outline of switched capacitance filters; non-linear circuits: logarithmic and antilogarithmic amplifier, ideal diode; stability of the resting point of an electronic circuit: exponential trigger and sinusoidal trigger and relationship with the position of the poles; (almost) sinusoidal oscillators: block diagram and operating principle; characteristics of the direct and feedback block, characteristic equation. descriptive function method; Wien bridge oscillator, phase shift oscillator, three-point oscillators (by Colpitts and

Hartley); negative differential resistors of type S and N and use in oscillators and multivibrators. monostable, astable and bistable multivibrator. Comparator and Schmitt trigger. Circuits with complex dynamics and chaos: ergodicity - mixingness - accuracy; Perron Frobenius operator and his properties; the case of a quantized state as a projection of the PF operator (equivalence with Markov chains). Outline of applications to EMI reduction in systems controlled by periodic signals and to the generation of random numbers.

9.3 PHD COURSES IN ITALIAN AND/OR FOREIGN UNIVERSITIES

I have also been responsible (or co-responsible) for some courses at Ph.D. level a reported in the following

- **PhD Course (20h)** on "Compressed Sensing: Theory, Circuits/Systems Implementation and Applications" for the PhD Students of the Department of Electronics and Telecommunications (DET), Politecnico di Torino, Turin, September 2023. The class has been fully flipped. Material is available at https://www.dropbox.com/sh/41tp1orohc34ff8/AAAC49fi1dZx9F6cu2c4Zya3a?dl=0 .
- **PhD Course (20h)** on "Compressed Sensing: Theory, Circuits/Systems Implementation and Applications" for the PhD Students of the Department of Electronics and Telecommunications (DET), Politecnico di Torino, Turin, September 2021. The class has been fully flipped. Material is available at https://www.dropbox.com/sh/41tp1orohc34ff8/AAAC49fi1dZx9F6cu2c4Zya3a?dl=0 .
- **PhD Course (6h)** on "Compressed sensing: theory and applications" for the PhD Students of the Department of Electronics and Telecommunications (DET), Politecnico di Torino, Turin, March 2019. Additional 14h are taught by Prof. Enrico Magli.
- **PhD Course (8h)** on "Analog Circuit Testing based on (Complex) Oscillations," for the PhD Students of the Department of Electrical Engineering, University of Washington, Seattle, June 2011.
- **PhD Course (16h)** on "Statistical Approach to Chaos with Applications to Information Technology" for the PhD Students of the European Doctorate in Information Technology (EDITH, see also Section on Research Projects), Bologna, November 2004.
- **PhD Course (12h)** on "Statistical Methodology for Studying Chaotic Systems: Theory and Applications to Optimize DS-CDMA Systems and EMI Reduction," for the PhD Students in Electrical Engineering, Faculty of Engineering, University of Naples "Federico II", March 2004.
- **PhD Course (16h)** on "Fundamentals of Statistical Analysis of Chaotic Circuits and Systems: Theory and Applications to Signal Processing and EMI Reduction," for the PhD Students in Information Engineering, Faculty of Engineering, University of Siena, September 2003.